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A Hybrid Heuristic Search Control Assisted Optimization of Dual-Input Doherty Power Amplifier

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***Abstract* — This paper proposes an auto-tuning approach to find the optimal configuration of a dual-input Doherty power amplifier (DIDPA) to enhance power efficiency while maintaining a good linearity level. The DIDPA configuration consists of a set of circuits and system-level parameters called free-parameters that are optimized through a hybrid heuristic search control (HHSC), which is the core of the auto-tuning approach. The HHSC convergence towards the optimal solution is conducted by a cost function designed to present a trade-off between efficiency and linearity. The HHSC was validated through experimental using a 20 MHz LTE signal at 3 GHz, where DIDPA exhibited a drain efficiency (DE) of 60% at an output power level of 36 dBm. The linearizability of DIDPA has been validated through digital predistortion (DPD), where the error vector magnitude (EVM) is reduced to 2.5%, and the adjacent channel power ratio (ACPR) is improved to -48 dBc.**

***Keywords* — dual-input Doherty power amplifier, optimization process, digital predistortion, crest factor reduction.**

I. Introduction

With the introduction of non-constant amplitude modulated signal in 4G LTE and 5G, the enhancement of power amplifier (PA) efficiency while maintaining an adequate linearity level becomes more challenging. For modulated signals with a high peak-to-average power ratio (PAPR), PA should operate at large power back-off, which decreases PA efficiency. Advanced PA architectures based on dynamic load or supply modulation have been proposed in the literature to avoid wasting excessive power resources. Some of the most popular solutions are Doherty PA, envelope tracking, and outphasing PA.

Although these architectures can be designed with a single RF input, several studies have been reported in the literature to highlight the benefits in maintaining separate inputs [1], and the advantages of dual-input Doherty PA (DIDPA) compared to single-input has been studied in [2]. Therefore, additional degrees of freedom, so-called free-parameters offered by the separate inputs, can be used to enhance the PA performance [3].

Focusing on DIDPA architecture, the search for the optimal free-parameters guaranteeing high performance requires experimental cross-validation, which is usually costly and computationally significant, especially when the search space is enormous. Nevertheless, identifying these free-parameters to their optimal values within a defined interval can be viewed as a global optimization problem.

The design and study of DIDPA with enhanced efficiency have been reported in many research works. Few of them deal with the joint optimization of DIDPA free-parameters and its linearization. The first related work is proposed in [4], where the authors used perturbed stochastic approximation (SPSA) algorithm to tune the free-parameters of DIDPA. In [5], the authors proposed a simulated annealing-based optimization to optimize the DIDPA. They applied a cost function including PAE, gain of DIDPA, output power P_{out} and ACPR as metric referring to the linearity. It is important to emphasize that no PAPR reduction or linearization technique was introduced in [5].

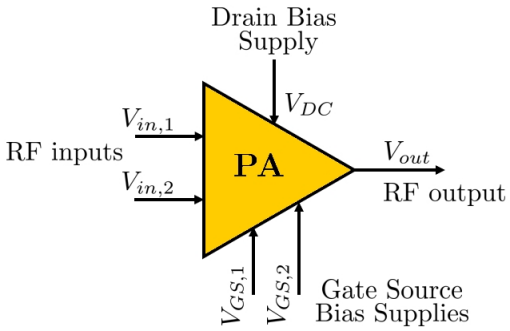


Fig. 1. Block diagram of dual-input Doherty PA.

In this paper, we proposed a novel auto-tuning approach to enhance the power efficiency of the DIDPA while meeting the linearity requirement. It consists of optimizing the free-parameters using a proposed hybrid heuristic search control (HHSC) according to a designed cost function that indicates the trade-off between power efficiency and linearity. The free-parameters cover PA biasing, power splitting, and PAPR reduction, such as crest factor reduction (CFR). A digital predistortion (DPD) based on an optimal low-complexity model is applied to meet the linearity requirements.

II. System-Level Aspects

A. Dual-Input Doherty Power Amplifier

The dual-input Doherty PA is illustrated in Fig. 1 has two RF inputs, a drain supply V_{DC} and two gate voltages V_{GS} to control the terminals of the main and peaking amplifiers independently.

The instantaneous amplitude and phase of each input in baseband, as well as the V_{GS} gate bias voltages, can be controlled and adjusted separately, which enable a large degree

of freedom to improve the performance of the PA, in particular its efficiency for varying input conditions.

In this paper, the DIDPA presented in [6] is used as the device under test (DUT).

B. Proposed Architecture

The optimization of DIDPA using HHSC is carried out within an architecture proposed in Fig. 2.

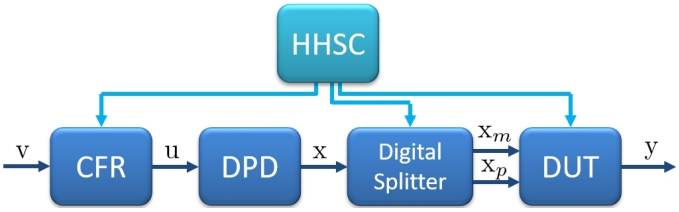


Fig. 2. Block diagram of the proposed architecture.

This architecture is consisting of 4 blocks:

- CFR is used to reduce the PAPR of $u(n)$ so that DIDPA can operate with less back-off.
- DPD linearizes DIDPA by compensating for its nonlinearities.
- Digital splitter is optimally designed to divide $x(n)$ into two different signals $x_m(n)$ and $x_p(n)$, since DIDPA requires two separate input signals for main and peaking amplifier.
- DUT represents DIDPA with its power supplies.

C. Free-Parameters

Each block in Fig. 2 has free-parameters to be set or controlled by HHSC, which are listed above.

1) Free-Parameter of CFR

The CFR technique used to reduce the PAPR is based on peak cancellation, the principle of which is based on the clipping and filtering CFR technique, and carried out through two stages: hard clip, and clip-and-filter.

Hard clip is the most basic CFR technique, where the input signal $v(n)$ is clipped according to a threshold μ. The signal generated at the first step is expressed as:

$$v_{HC}(n) = \begin{cases} v(n) \times \left(1 - \frac{\mu}{|v(n)|}\right) & \text{if } |v(n)| \geq \mu \\ v(n) & \text{if } |v(n)| < \mu \end{cases} \quad (1)$$

At the second stage, $v_{HC}(n)$ is filtered using noise shaping. Finally, the output signal $u(n)$ is given by subtracting a time-aligned weighted version of the filtered peak cancellation signal from the original input signal $v(n)$.

$$u(n) = v(n-d) - \alpha_s \times \text{filter}\{v_{HC}(n)\} \quad (2)$$

where α_s is the subtraction parameter.

Therefore, we use the clipping threshold μ as a free-parameter of CFR block to be controlled.

2) Free-Parameters of Digital Splitter

The motivation behind using two separate RF inputs is to eliminate analog input splitters, such as Wilkinson divider, and to allow independent power control to the main and peaking amplifier.

Digital splitter divides the complex signal $x = Xe^{j\theta}$ into two complex signals x_m and x_p defined as:

$$x_m = \alpha_m x \ ; \ x_p = \alpha_p e^{-j\phi} x \quad (3)$$

We propose to take the power ratio α and the phase offset ϕ as free-parameters with

$$\alpha_m = \sqrt{\alpha} \ ; \ \alpha_p = \sqrt{1-\alpha} \quad (4)$$

3) Free-Parameters of DUT

The main and peaking inputs of DIDPA control the main and peaking amplifier, biased with $V_{GS,m}$ and $V_{GS,p}$, respectively. Since these biased voltages are controlled from baseband, they will be taken as a free-parameters to be optimized by HHSC within a range of DC voltage.

4) Free-Parameters of DPD

In this architecture, DPD will not be controlled by HHSC since the DPD technique requires estimating the model coefficients by involving linear regression techniques such as the least-square (LS) method. DPD is operated separately.

III. Hybrid Heuristic Search Control

The principle of HHSC is based on combining simulated annealing (SA) [7] as a global optimization search and extremum-seeking control (ESC) [8] as an adaptive control to fine-tune the optimized results. The algorithm of HHSC is described in Algorithm (1). The free-parameters vector to be optimized is defined by $\Theta = [\mu; \alpha; \phi; V_{GS,m}; V_{GS,p}]$ The cost function corresponding to Θ is denoted by $J(\Theta)$. The optimal solution is denoted by $\Theta_{\text{opt,HHSC}}$.

The cost function J is designed to ensure a good trade-off between linearity and efficiency. The linearity requirement is presented by 2 figures of merit (FOMs): error vector magnitude (EVM) and adjacent channel power ratio (ACPR), while the efficiency requirement is presented by 2 FOMs: the power-added efficiency (PAE) and the output power P_{out} of DIDPA. It is defined by the normalized weighted sum method in (5) with constraints in (6).

$$J = \sum_i w_i \left| \frac{\text{FOM}_i}{\text{FOM}_{t,i}} \right| \quad i = \{1,2,3,4\} \quad (5)$$

where w_i is the weighting coefficient corresponding to FOM_i, and $\text{FOM}_{t,i}$ is the target value that the user attempts to reach. The FOMs used here are $\{\text{EVM;ACPR;PAE;P}_{out}\}$

The constraints on J are defined as:

$$\sum_{i=1}^{4} w_i = 1 \quad \text{and} \quad \max \left| \frac{\text{FOM}_i}{\text{FOM}_{t,i}} \right| = 1 \quad (6)$$

Algorithm 1: Algorithm of SA and ESC

Initialization: $\mathcal{T}_0$, $\mathcal{T}_f$, $iter = 0$, $\mathcal{K}$, a, ω, SA_{max}
Initial random solution Θ_0
$\Theta = \Theta_0$ and $\Theta_{\text{opt,SA}} = \Theta$
Evaluate $J(\Theta)$
$\mathcal{T} = \mathcal{T}_0$
while $\mathcal{T} > \mathcal{T}_f$ **do**
  while $iter < SA_{max}$ **do**
    $iter = iter + 1$
    Select a random neighbor Θ' in neighbrhood space $\Psi(\Theta)$
    $\Delta E = J(\Theta') - J(\Theta)$
    if $\Delta E > 0$ **then**
      $\Theta = \Theta'$
      if $J(\Theta')$ *is better than* $J(\Theta_{opt,SA})$ **then**
        $\Theta_{\text{opt,SA}} = \Theta'$ and $J_{\text{opt,SA}} = J(\Theta')$
      end
    else
      Generate random $r \in [0\ 1]$
      if $r < e^{\frac{-\Delta E}{\mathcal{T}}}$ **then**
        $\Theta = \Theta'$
      end
    end
  end
  $\mathcal{T} = \mathcal{C} \times \mathcal{T}$
  $iter = 0$
end
$\Theta_{\text{0,ESC}} = \Theta_{\text{opt,SA}}$
$\Theta = \Theta_{\text{0,ESC}}$
$J_{old} = J_{\text{opt,SA}}$
while *1* **do**
  Evaluate $J(\Theta)$
  if $J(\Theta) > J_{old}$ **then**
    $J_{old} = J(\Theta)$
    $\xi = J(\Theta) \times a\sin(\omega t)$
    $\Theta = K \times \int \xi + a\sin(\omega t)$
  else
    $\Theta_{\text{opt,HHSC}} = \Theta$
    $J_{\text{opt,HHSC}} = J(\Theta_{\text{opt,HHSC}})$
    end While loop
  end
end
Return $\Theta_{\text{opt,HHSC}}$

The design in (5) and (6) is made such that HHSC attempts to maximize J to 1, indicating that the user's specifications are met. In this way, we give the cost function a logical interpretation since the different FOMs do not have the same meaning or same unit.

IV. Experimental Test Bench

HHSC is validated through experiments that have been carried out using a test bench in Fig. 3.

The baseband IQ data are generated and split into two different IQ data inputs sent to the DUT through AD9371 dual-channel RF transceiver, which up-converts the baseband signals to the carrier frequency f_c at 3 GHz. For the observation path, The RF output signal is down-converted to baseband by AD9371, which provides the baseband signal to the PC workstation. Around 100,000 IQ samples were recorded for the baseband process with a sampling rate at 245.76 MSPS.

Fig. 3. Test bench of DIDPA.

The DIDPA is tested using a 64-QAM 20 MHz LTE signal with a roll-off factor of 0.6 and a PAPR of 8.2 dB.

V. Experimental Results and Discussion

First, we set the search range of the free-parameters to be optimized, which are summarized in Table 1, based on raw estimation.

Table 1. Free-parameters of the proposed architecture.

Bloc	Free-parameter	Search Range	Unit
CFR	μ	[0 2]	dB
Digital splitter	α	[0 1]	–
	ϕ	[-180 20]	Degree
DUT	$V_{GS,m}$	[-4 -1]	Volt
	$V_{GS,p}$	[-4 -1]	Volt

In this test, the target FOMs defined at user's specification are defined by EVM_t=3%, ACPR_t=-50 dB, PAE_t=100%, and $\text{P}_{out,t}$=40 dBm. The weighting coefficients corresponding to target FOMS are initialized as $[w_1; w_2; w_3; w_4] = [0.1; 0.1; 0.4; 0.4]$.

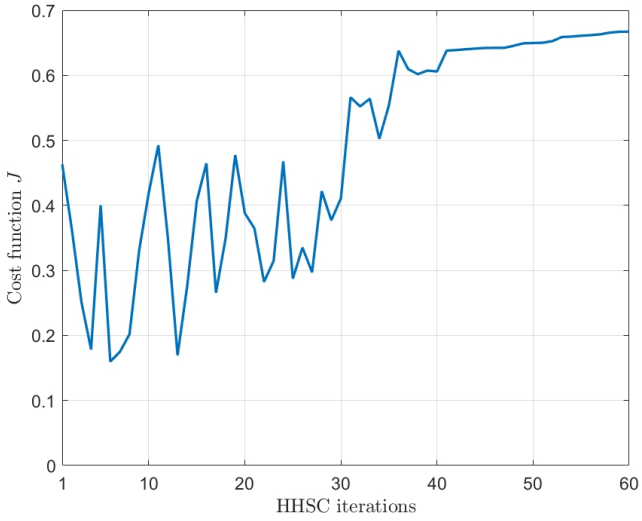


Fig. 4. Evolution of cost function J over HHSC iterations.

We attribute more weights to the efficiency FOMs since DPD will be included to linearize the DUT. This refers to the fact that the linearity requirements are more relaxed, as it is relatively easier to meet with DPD, unlike efficiency.

According to Algorithm (1), HHSC is performed starting from an initial $\Theta_0 = [0\text{dB}\ 0.5\ \ -90^\circ\ \ -1.5\text{V}\ \ -2.5\text{V}]$, and converges towards $\Theta_{\text{opt,HHSC}} = [1.1\text{dB}\ 0.7\ -135^\circ\ -1.33\text{V}\ -2.87\text{V}]$. The convergence of J is shown in Fig. 4.

The FOMs corresponding to $\Theta_{\text{opt,HHSC}}$ are summarized in Table 2. Efficiency FOMs are enhanced by sacrificing the linearity FOMs. This confirms the choice of the initial weighting coefficients where w_3 and w_4 have more influence than w_1 and w_2.

Table 2. FOMs according to the optimal free-parameters $\Theta_{\text{opt,HHSC}}$.

EVM	ACPR	PAE	DE	P_{out}	Gain
10.63%	-27dB	59.29%	62%	36 dBm	15.5 dB

DPD is incorporated to evaluate the linearizability of the DIDPA under $\Theta_{\text{opt,HHSC}}$. The DPD model is based on a decomposed vector model (DVR) model [9] and optimally sized using Hill Climbing heuristic [10]. The number of model coefficients is limited to 30 coefficients making it a low-complex model. Fig. 5 presents the improvement of ACPR to -48 dBc, at an average output power of 34 dBm with DE of 50%. The EVM improvement is illustrated in Fig. 6 from 10% to 2.5%, where the IQ constellation before and after DPD are shown. Our approach can be applied multi-input advanced PA to optimize the system-level performance including linearity.

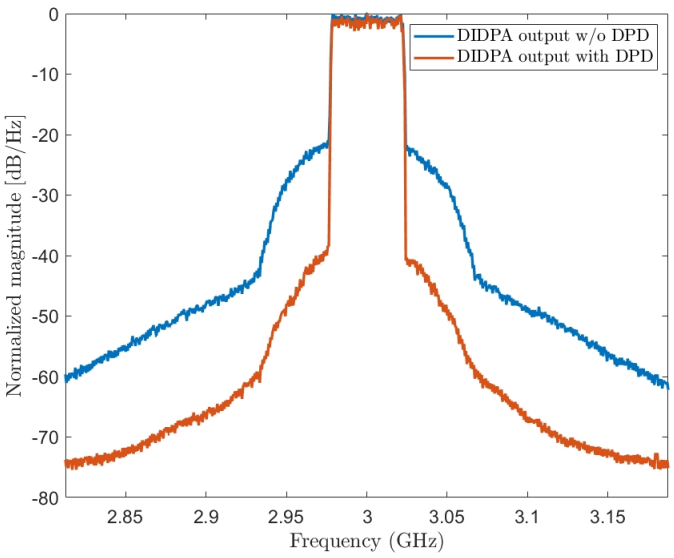
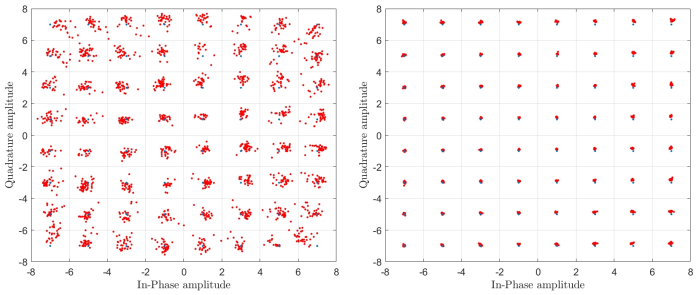


Fig. 5. Spectra of the output signal of DUT without and with DPD.

VI. Conclusion

In this paper, a novel auto-tuning approach is proposed to exploit DIDPA to maximize power efficiency while being compliant with the linearity specifications. This approach relies on conducting a global optimization combined with a control process to find the optimal free-parameters according to a designed cost function, representing the trade-off between efficiency and linearity. In the experiments, the user's specification are met when DPD is applied to linearize DIDPA under the optimal configuration with outstanding results. Our approach can also be applied to other multi-input advanced PA architectures to improve the system-level performances including linearity.



(a) (b)

Fig. 6. IQ constellation: (a) Without DPD; (b): With DPD

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