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Abstract

GaN technology is not only gaining traction in power and RF electronics but is rapidly expanding into other application areas including digital and quantum computing electronics. This paper provides a glimpse of future GaN device technologies and advanced modeling approaches that can push the boundaries of these applications in terms of performance and reliability. While GaN power devices have recently been commercialized in the 15-900 V classes, new GaN devices are greatly desirable to explore both the higher-voltage and ultra-low-voltage power applications. Moving into the RF domain, ultra-high frequency GaN devices are being used to implement digitized power amplifier circuits, and further advances using hardware-software co-design approach can be expected. On the horizon is the GaN CMOS technology, a key missing piece to realize the full-GaN platform with integrated digital, power and RF electronics technologies. Although currently a challenge, high-performance p-type GaN technology will be crucial to realize high-performance GaN CMOS circuits. Due to its excellent transport characteristics and ability to generate free carriers via polarization doping, GaN is expected to be an important technology for ultra-low temperature and quantum computing electronics. Finally, given the increasing cost of hardware prototyping of new devices and circuits, the use of high-fidelity device models and data-driven modeling approaches for technology-circuit co-design are projected to be the trends of the future. In this regard, physically inspired, mathematically robust, less computationally taxing, and predictive modeling approaches are indispensable. With all these and future efforts, we envision GaN to become the next Si for electronics.

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Emerging GaN technologies for power, RF, digital, and quantum computing applications: recent advances and prospects

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GaN technology is not only gaining traction in power and RF electronics but is rapidly expanding into other application areas including digital and quantum computing electronics. This paper provides a glimpse of future GaN device technologies and advanced modeling approaches that can push the boundaries of these applications in terms of performance and reliability. While GaN power devices have recently been commercialized in the 15-900 V classes, new GaN devices are greatly desirable to explore both the higher-voltage and ultra-low-voltage power applications. Moving into the RF domain, ultra-high frequency GaN devices are being used to implement digitized power amplifier circuits, and further advances using hardware-software co-design approach can be expected. On the horizon is the GaN CMOS technology, a key missing piece to realize the full-GaN platform with integrated digital, power and RF electronics technologies. Although currently a challenge, high-performance p-type GaN technology will be crucial to realize high-performance GaN CMOS circuits. Due to its excellent transport characteristics and ability to generate free carriers via polarization doping, GaN is expected to be an important technology for ultra-low temperature and quantum computing electronics. Finally, given the increasing cost of hardware prototyping of new devices and circuits, the use of high-fidelity device models and data-driven modeling approaches for technology-circuit co-design are projected to be the trends of the future. In this regard, physically inspired, mathematically robust, less computationally taxing, and predictive modeling approaches are indispensable. With all these and future efforts, we envision GaN to become the next Si for electronics.

I. INTRODUCTION

GaN devices have increasingly gained wider acceptance as a technology that demonstrates numerous strengths for applications in power electronics,[1] RF,[2,3] and more lately in the areas of digital and ultra-high and ultra-low temperature electronics.[4] A major strength of the GaN technology is its unique ability to operate in both very high and very low temperature environments. Due to its unique material attributes, including wide bandgap and excellent transport parameters, GaN can meet the high temperature, high frequency, and high power demands of various industrial applications[5,6] including deep well drilling, automobile, and aerospace. At the same time, GaN-based devices can operate in very low temperature environments that are relevant for superconducting and quantum computing applications. Due to its polarization-induced doping, GaN can overcome the carrier freeze-out challenges of other technologies such as doped silicon.[7,8]

Power semiconductor industry focuses on a wide gamut of applications ranging from lighting, power grid, to automobile, etc. Currently, GaN high electron mobility transistor (HEMT) products have been commercialized for operation in the 15–650 volts range.[1,3,9] Compared to Si, GaN HEMTs offer much higher switching frequency and are thus widely adopted for high-speed and wireless charging and electrified transportation. Vertical GaN power devices on native substrates are close to commercialization,[10,11] whereas vertical structures fabricated on foreign substrates, such as low-cost silicon, sapphire, and engineered substrates, are also being investigated. In addition to the high-voltage products, GaN technology also provides unique opportunities for ultra-low voltage products (e.g., below 15 V).[11] A new generation of GaN devices based on the concept of superjunctions has shown tremendous benefits for power applications.

Currently, RF is the next best-known application of the GaN technology. GaN-based power amplifiers (PAs) offer significantly enhanced RF performance (i.e., power density and bandwidth) compared to those based on legacy technologies. To further push the PA efficiency and bandwidth for mm-wave operation, the digitization of the PA and the hardware-software co-design at the device and circuit levels are discussed. At the device level, novel epitaxial heterostructures and architectures, such as vertical device designs that leverage

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the knowledge gained from power electronics applications of GaN, could provide better thermal distribution, higher breakdown voltages, and power density compared to lateral structures. We also briefly discuss the innovations such as 3D electron gas graded-channel devices,[12] FinFET technology[13] and, the digital GaN CMOS technology,[14] to enhance the RF linearity.

For digital and ultra-low-temperature applications, GaN provides substantial advantages compared to silicon and III-V technologies. The wide bandgap of GaN suppresses band-to-band tunneling and gate-induced drain leakage, thus reducing the static power dissipation. However, there are still a number of challenges to address, one of which is the lack of high-performance p-FET GaN, a necessary technology for the practical realization of CMOS circuitry. The other challenge pertains to the high defect density of GaN-on-Si wafer, but engineered substrates are expected to yield better results.

Quantum computing electronics is the next frontier of GaN technology applications. Breakthroughs can be expected from the progress made in qubit management and associated components with the potential for large-scale hardware integration or/and "quantum computing-on-chip".[15,16] We see exciting new avenues of research in cryogenic GaN CMOS electronics for the control and readout operation in quantum computing and the use of nitrogen vacancy (NV) centers in III-nitride technology as robust qubits.

This paper wraps up with a discussion on the modeling of GaN devices, emphasizing the viewpoint that modeling could serve as a tool to complement the traditional experimental approaches in the study of performance and reliability. Given that GaN devices are generally limited by degradation mechanisms, especially those introduced by traps and mechanical and thermal stresses, there is a need to develop modeling frameworks that integrate the physics of reliability with carrier dynamics. Additionally, research and development of circuit-compatible compact device models and process design kits are imperative to enable the co-design and co-optimization of materials-devices-circuits-software and enable the cross-fertilization of distinct GaN technologies. Ultimately, we expect such innovations to push GaN to new technological heights and enable its deployment in new and emerging commercial applications.

II. GAN FOR POWER ELECTRONICS

A. Current Status

Power semiconductor devices are utilized as solid-state switches in power electronics systems that are ubiquitous in consumer electronics, data centers, electric vehicles, electricity grid, and renewable energy systems. The global power semiconductor market is predicted to reach over $50 billion by the end of 2025.[17] Power electronics applications span a wide range of voltage, current, and power classes. Some representative applications are shown in Fig. 1. Power devices with a rated voltage < 650 V, 650-1700 V, and > 1700 V are usually categorized as the low-voltage (LV), medium-voltage (MV), and high-voltage (HV) devices, respectively. Note that different boundaries may be used in the context of power applications, e.g., MV applications span voltages up to 10-35 kV. Regardless of voltage/current classes, the common power device design centers around the concurrent realization of low on-resistance (R_{ON}), high breakdown voltage (BV), and small turn-on/turn-off power losses (i.e., switching losses). The trade-offs between these metrics hinge on both material properties and device structures.

To date, three power semiconductor materials have reached massive production and commercialization, i.e., Si, silicon carbide (SiC), and GaN. A variety of Si devices are available throughout all voltage classes. SiC Schottky barrier diodes (SBDs) and MOSFETs have been commercialized in the 650-1700 V classes, with engineering samples available up to 10 kV. Very recently, the GaN HEMT has been commercialized in the 15-650 V classes,[1,3,9] and its market size is projected to exceed $1.25 billion by 2027.[18] Owing to GaN's superior physical properties over Si and SiC for power applications, GaN HEMTs allow for higher switching frequency and, therefore, have already seen wide adoptions in fast chargers, wireless charging, data centers, and electrified transportation. The higher frequency allows the miniaturization of passive components in power systems, enabling higher power density and conversion efficiency, as well as a reduction in system volume and weight. Additionally, all commercial GaN HEMTs rely on large-diameter GaN-on-Si wafer and can be produced in CMOS-compatible processes, suggesting a lower wafer and processing cost compared to the SiC counterparts.[19]

Currently, four main structures are adopted in commercial GaN HEMTs, as illustrated in Fig. 2. While all of them employ the two-dimensional electron gas (2DEG) channel, their main difference lies in the gate stack, or more specifically the techniques to enable the enhancement-mode (E-mode) operation, which is highly desirable for power electronics applications. The Schottky-type p-gate HEMT (SP-HEMT) (Fig. 2(a)) and gate injection transistor (GIT) (Fig. 2(b)) both use p-GaN to deplete the 2DEG under the gate, but they feature different contacts between the gate metal and p-GaN. The recessed gate and Ohmic gate contact in the GIT favor the hole injection and conductivity modulation, which are not present in the SP-HEMT. The cascode (Fig. 2(c)) and direct-drive devices usually co-package a high-voltage depletion-mode (D-mode) GaN HEMT with a low-voltage E-mode Si power MOSFET to make the composite device function like a single high-voltage E-mode transistor. Direct-drive devices also co-package the gate driver and protection Si ICs with the GaN and Si power transistors.

This section aims at discussing recent efforts for expanding the application space of GaN power devices. First, extensive research emphasizes on developing new GaN devices beyond the 15-650 V range. With the advent and maturity of large-diameter, low-dislocation GaN wafers on freestanding GaN substrates,[20] a new generation of vertical GaN power devices has been demonstrated with a BV up to 2 kV in transistors[21] and 5 kV in p-n diodes.[22] In addition to operating at higher voltages, the vertical device allows spatially distributed current and electric field, which facilitates the power scaling and

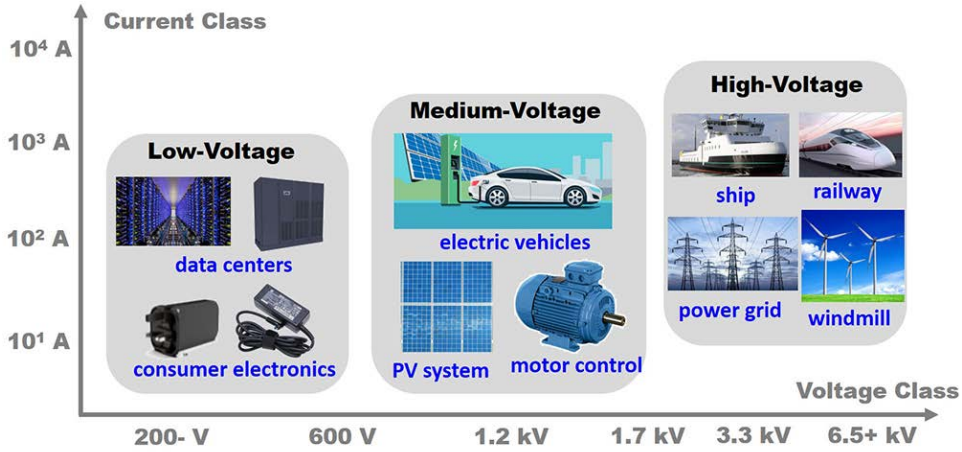

FIG. 1: Representative applications of power electronics applications.

thermal management. Inspired by the efficacy of power scaling through current spreading, MV/HV lateral GaN devices with stacked 2DEG channels have also been demonstrated with high performance up to 5-10 kV.[23,24] These emerging vertical and lateral MV/HV GaN devices will be discussed in Sec. II B.

Meanwhile, the 3-D FinFET and trigate architectures have been innovatively employed in both lateral and vertical GaN devices.[9] Very different from Si digital FinFETs, GaN FinFETs and trigate devices have allowed for numerous structural innovations based on engineering 2DEG and a variety of gate stacks based on metal-insulator-semiconductor (MIS) structures or p-n junctions.[9] Some of these GaN trigate devices show good promise for expanding the GaN's application space into the ultra-low-voltage power electronics (e.g., below 15 V). These devices will be presented in Sec. II C.

The penetration of GaN into power electronics not only hinges on developing new GaN devices but also on expanding the deployment of existing GaN devices. For example, in electric vehicles (EV), power electronics are employed for charging the batteries from the utility grid and running the motors.[25] Power devices are used mainly in three systems, i.e., on-board charger, DC/DC converter, and traction inverter. The performance of the first two systems could be significantly boosted by a higher switching frequency; hence, GaN HEMTs are penetrating fast into these markets. Differently, the powertrain inverter, the market size of which is the highest among the three, does not require aggressive frequency upscaling due to the motor load. Instead, prioritized device considerations are high power density, excellent reliability, and good robustness under abnormal operations.[25] The reliability and ruggedness of GaN HEMTs under surge energy, short current, overvoltage, and overcurrent events, as well as the device metrics (e.g., R_{ON}, BV) under fast switching, were found to be impacted by the time-dependent trapping and de-trapping phenomena uniquely present in GaN HEMTs. These issues will be discussed in Sec. II D.

Finally, in Sec. II E, based on the progress detailed in previous sections, we provide a prospect for the development of GaN superjunction devices. The superjunction has achieved huge success in Si and can elevate the performance of GaN power devices to a new level.

B. Medium- and High-Voltage GaN Devices: Vertical or Lateral?

The vertical structure is often believed to favor high-voltage, high-power devices as it facilitates current spreading and thermal management[26] and allows for the realization of high voltage without enlarging the chip size.[20] Almost all commercial MV/HV Si and SiC power devices are based on the vertical structure.[21] Additionally, as compared to the GaN-on-Si epitaxy, GaN-on-GaN homoepitaxial layers possess a much lower dislocation density, which favors the reduction of off-state leakage current and the enhancement of BV. Over the last several years, the cost of GaN-on-GaN wafer is dropping fast, and 4-inch freestanding wafer is widely available now.[19]

The studies of vertical GaN devices started from p-n diodes, as the p-n junction is a key building block for many advanced power devices. Multiple groups have reported 3.3 kV-5 kV GaN p-n diodes with a differential-R_{ON} v.s. BV trade-off exceeding the 1-D SiC unipolar limit.[22,27–29] The avalanche capability, a non-destructive breakdown process that allows power device to accommodate large current at BV, has been widely demonstrated in vertical GaN p-n diodes.[28–32] State-of-the-art avalanche performance in an industry 1.7 kV GaN p-n diode shows an avalanche current and avalanche energy of 51 A and 63 mJ, respectively.[31] In p-n diodes, a breakdown field of 2.8-3.5 MV/cm close to intrinsic GaN limits has also been demonstrated.[33] Industrial vertical GaN p-n diodes also demonstrated a surge current ruggedness close to the state-of-the-art SiC counterparts, while showing smaller reverse recovery and faster switching speed.[32]

However, the vertical GaN p-n diode may not be competitive as a standalone power rectifier due to the large turn-on voltage (V_{ON}) resulting from the large bandgap of GaN. Advanced SBDs are highly desirable, as they combine a

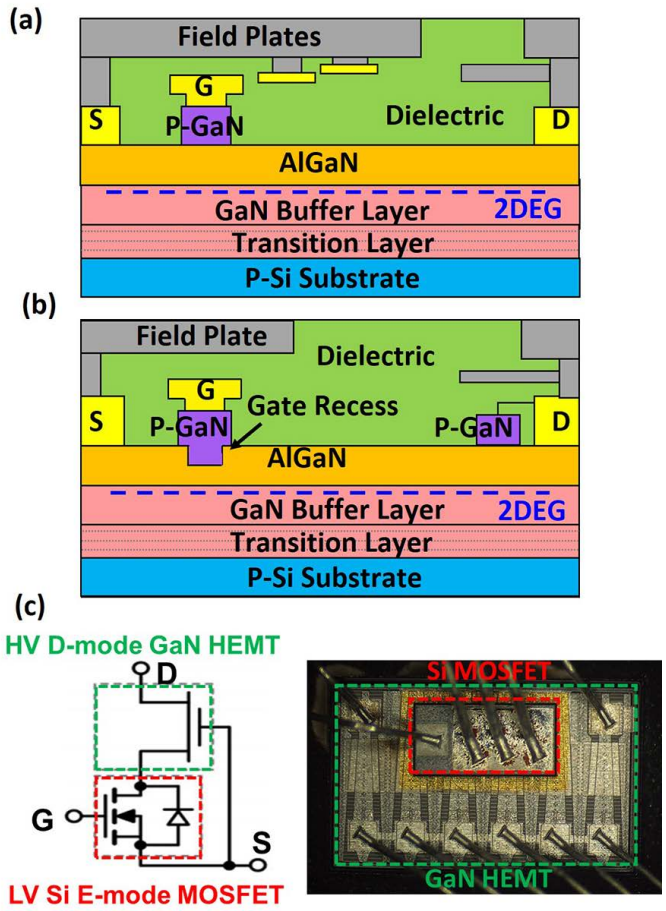

FIG. 2: Schematic or decapped photos of four mainstream commercial GaN HEMTs: (a) SP-HEMT, (b) GIT, and (c) cascode GaN HEMT.

Schottky-like forward characteristics (with a low V_{ON}) and a pn-like reverse characteristics (with the peak electric field moved into semiconductor from the surface). These advanced SBDs include the trench MIS/MOS barrier Schottky (TMBS) diode (Fig. 3(a)), the junction barrier Schottky (JBS) diode (Fig. 3(b)), and the merged p-n/Schottky diode (MPS). These diodes employ either the MIS stack or the p-n junction to deplete the top part of the drift region at low reverse biases, thereby shielding the top Schottky contact from high electric field. The JBS and MPS diodes have a similar structure and only differ in the Schottky or Ohmic contact to p-GaN. 600-700 V GaN TMBS diodes[34] and JBS diodes[35], as well as 2 kV MPS diodes,[36] have exhibited at least 100-fold lower leakage current compared to standard SBDs. Toyoda Gosei reported an industrial 10-A, 750-V GaN TMBS diode operational at over 200°C[37] in converter applications.[38]

Several 1.2-kV-class vertical GaN transistors have been demonstrated with a BV up to 2 kV[21] and current up to 100 A,[10] and a few industry devices[10,38–41] of such, are close to commercialization. The current-aperture vertical electron transistor (CAVET)[39,42–44] (Fig. 4(a)) relies on the 2DEG channel and utilizes buried p-GaN regions to confine the current flow in an aperture for gate control. The CAVET is intrinsically depletion-mode (D-mode), but a trench semi-polar gate[39,42] or a p-GaN gate[43] can enable the enhancement-mode (E-mode) operation. The GaN trench MOSFET[10,45,46] (Fig. 4(b)) is very similar to the Si and SiC counterparts and relies on inversion-type MOS channel. A variant of the trench MOSFET, the in situ oxide, GaN interlayer-based trench MOSFET (OG-FET),[47–49] introduces a regrown, thin, unintentionally-doped GaN interlayer to convert the inversion-type MOS channel into the accumulation-type MOS channel while maintaining the E-mode operation. The vertical GaN planar power MOSFET[50] similar to the SiC counterpart[51] has also been demonstrated with a BV over 1.2 kV.

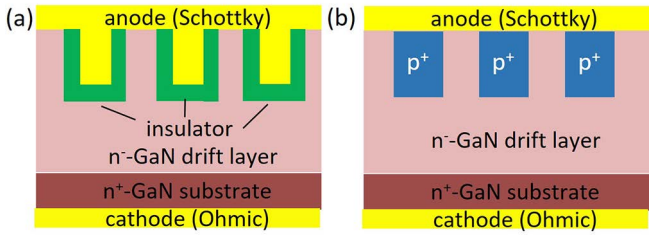

FIG. 3: Schematic of vertical GaN (a) TMBS and (b) JBS rectifiers.

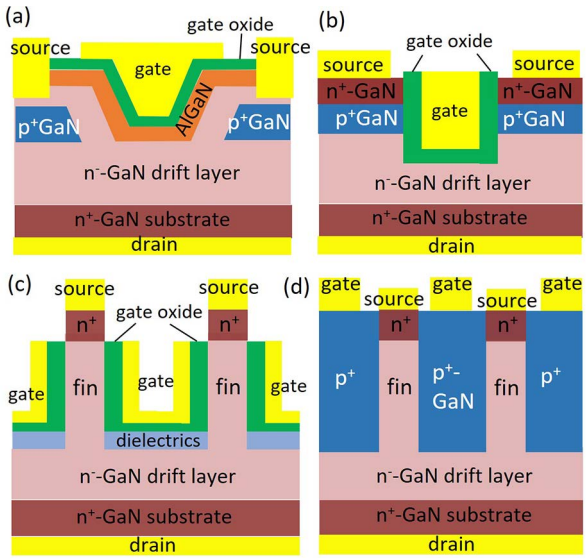

FIG. 4: Schematic of vertical GaN (a) CAVET, (b) trench MOSFET, (c) Fin-MOSFET, and (d) Fin-JFET.

The vertical GaN FinFETs[11,21] leverage the digital FinFET concept and employ the submicron-meter fin-shaped channels to provide superior gate control as well as to enable the E-mode operation and bidirectional conduction. The small footprint of fin channels allows much higher channel density as compared to conventional power MOSFETs. Depending on the sidewall gate stack, there are two types of power FinFETs, the Fin-MOSFET (Fig. 4(c) and Fin-JFET (Fig. 4(d)).[11,21] In each fin, the Fin-MOSFET features a bulk fin channel in par-

allel with two sidewall accumulation-type MOS channels,[52] and the device needs only n-type GaN.[53] In the Fin-JFET, the inter-fin region is filled with p-GaN, and the strong depletion of the lateral p-n junction allows a high doping concentration in the n-GaN fin while maintaining the E-mode operation.[40,41] 1.2 kV vertical GaN Fin-MOSFETs[54,55] and Fin-JFETs[40,41] have both shown 3-5 fold lower specific R_{ON} and superior switching performance[40,55] as compared to the state-of-the-art 1.2 kV SiC MOSFETs. An industrial GaN Fin-JFET for the first time demonstrates the avalanche capability in GaN transistors, with an avalanche energy density comparable to SiC MOSFETs.[40,41]

In addition to free-standing GaN substrates, vertical GaN devices can be also fabricated on low-cost foreign substrates, such as Si, sapphire, and engineering substrates (e.g., QST).[19] The relevant studies date back to the first demonstration of vertical GaN-on-Si diodes using a quasi-vertical structure[56] (Fig. 5(a)). Fully-vertical GaN-on-Si devices were later developed by a variety of approaches to handle the insulative, defective transitional layers, including the layer transfer[57,58] (Fig. 5(b)), buffer doping[59,60] (Fig. 5(c)), and deep backside trenches[61] (Fig. 5(d)). The state of the art includes 500-800 V vertical GaN-on-Si diodes[61,62] and MOSFETs[63] as well as 1.4 kV vertical GaN-on-sapphire SBDs.[64] The BV is expected to be increased fast with the recent availability of thick GaN (>10 μm) epi on Si substrates[65] and engineering substrates.[66]

The development of vertical GaN device on foreign substrates is still at an early stage, and many open questions remain. A key question is the cost and performance trade-offs for vertical GaN devices on different substrates. GaN on sapphire and Si can allow for much lower epitaxial cost as compared to GaN on GaN at the price of a higher dislocation density.[19] For example, the typical dislocation densities in GaN on GaN, sapphire, and Si are $10^3 \sim 10^6$ cm^{-2}, $10^7 \sim 10^8$ cm^{-2}, and $10^8 \sim 10^9$ cm^{-2}, respectively. The higher dislocation density in GaN-on-Si were found to induce a relatively small degradation in forward characteristics but a higher OFF-state leakage current at high biases.[67,68] Interestingly, although the BV of vertical GaN-on-Si devices is often governed by a trap-mediated process,[19] this trap-mediated BV was reported to retain an avalanche ruggedness in the switching circuit.[31,69] The impact of traps on the device leakage and breakdown, as well as their correlations with different fabrication techniques to enable the fully-vertical GaN-on-Si and GaN-on-sapphire device, need to be scrutinized by future research in device, materials, and physics. In addition, in vertical GaN devices on foreign substrates, the impact of higher leakage current on device reliability and robustness has not yet been understood. Note that this understanding is also important for lateral GaN-on-Si power and RF devices, as their leakage current at high drain bias is primarily vertical through the GaN buffer layer and transition layers. While all commercial GaN-on-Si devices have shown excellent reliability qualification data, there seems lacking a fundamental and comparative study into the impact of substrate selection (and GaN dislocation density) on the reliability and robustness of lateral GaN devices. On the other hand, it should be noted that the good reliability of commercial GaN-on-Si lateral HEMTs does not necessarily suggest a comparable reliability in vertical GaN devices on foreign substrates, as the major carrier transport direction is completely different in these two types of devices.

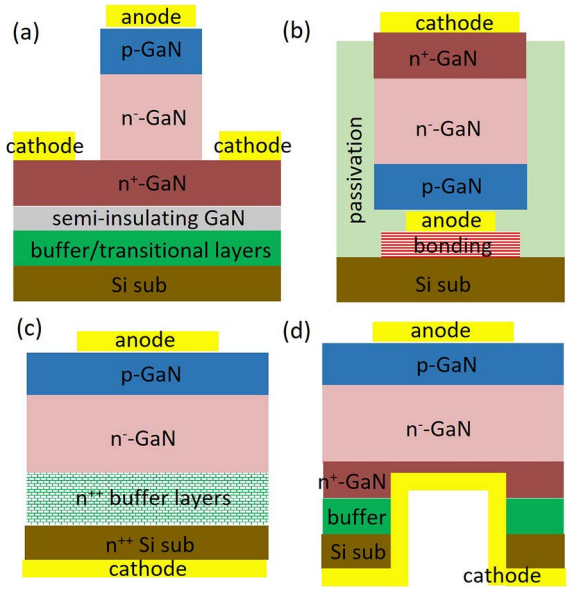

FIG. 5: Schematic of (a) quasi-vertical GaN-on-Si diodes and the fully-vertical diodes through (b) layer transfer, (c) buffer doping, and (d) selective removal of substrate and buffer layers.

While the vertical structure is undoubtedly suitable for MV/HV devices, the recent availability of large-diameter AlGaN/GaN wafers with multiple stacked 2DEG channels opens a new route for developing MV/HV GaN devices. The 2DEG mobility is higher than the bulk GaN mobility. Meanwhile, the stacked 2DEG channels allow significantly lower sheet resistance (R_{SH}) and higher current (and power) handling capabilities as compared to the single-channel counterpart. Multi-channel AlGaN/GaN SBDs[70] and HEMTs[71] up to a BV of 900 V and 1.2 kV, respectively, have been demonstrated with a tri-gate structure, i.e., the multi-2DEG fins being wrapped by MIS structures in the anode/gate regions. These multi-channel MV devices have shown significantly lower specific R_{ON} as compared to the single-channel counterpart.

Inspired by the electric field robustness of p-n junctions in vertical devices, a p-GaN based edge termination (Fig. 6(a)) was proposed for electric field management in multi-channel lateral devices,[72] which has enabled HV 5-channel SBDs up to 5 kV on the large-diameter, low-cost GaN-on-sapphire wafers.[24,72] Compared to the conventional field-plate termination (Fig. 6(b)), the p-GaN termination has no dielectrics/GaN interfaces, is not sensitive to geometrical designs, and its fabrication is compatible to the p-GaN HEMT foundry process. Additionally, the p-GaN termination allows hole injection and thus can potentially enable a superior ruggedness. 1.65-3.35 kV p-GaN-terminated multi-channel AlGaN/GaN SBDs show a R_{ON} v.s. BV performance superior to the 1-D unipolar SiC limit.[72] Subsequently, a novel junction-fin-anode was pro-

posed that wraps p-n junctions around the multi-2DEG fin (Fig. 6(c), (d)), where p-NiO was used to form conformal p-n junctions.[24] Benefiting from the strong depletion provided by this 3-D junction-fin-anode, the leakage current of a 5-channel SBD at multi-kilovolts is equal to that of a single-channel sidewall SBD biased at a few volts.[24]

Very recently, the first 10-kV class GaN device was demonstrated on the multi-channel AlGaN/GaN platform[23]. The 10-kV SBD employs a new E-field management design, the p-GaN reduced surface field (RESURF) structure, which is located on top of the multi-channel (Fig. 6(e)). Compared to the p-GaN termination, the p-GaN RESURF layer extends to the region nearing the cathode, and its total acceptor charges balance the net donor charges in the multi-channel structure (Fig. 6(f)). Thanks to this charge-balance design, the SBD with a 123 μm anode-to-cathode distance shows a BV over 10 kV and a R_{ON} of 39 mΩ·cm^2 (normalized with the device active region taking into account the contact transfer/extension lengths), which is 2.5-fold lower than the R_{ON} of the state-of-the-art 10-kV SiC JBS diodes.

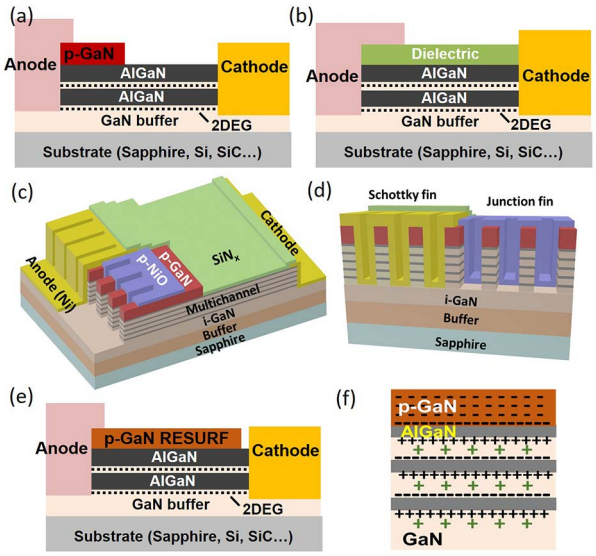

FIG. 6: Schematic of multi-channel diodes with (a) p-GaN termination and (b) field-plate termination. 3-D (c) side-view schematic and (d) cross-sectional view of a multi-channel AlGaN/GaN SBD with the junction-fin-anode. Schematic of (e) the RESURF multi-channel diode, and (f) the charge balance in the structure.

As a summary of Session IIB, the R_{ON} v.s. BV trade-offs of the state-of-the-art GaN MV/HV devices, as well as SiC devices for comparison, are plotted in Fig. 7. Also included are the 1-D unipolar limit of vertical Si, SiC, and GaN devices (assuming a mobility of 1000 cm^2/Vs in vertical GaN), as well as the practical limit of single-channel and multi-channel lateral GaN devices[72] (assuming a sheet resistance, R_{SH}, of 115 Ω/sq for multi-channel and 300 Ω/sq for single-channel devices, as well as an average anode-to-cathode/gate-to-drain electric field of 1 MV/cm). As shown in Fig. 7, state-of-the-art GaN MV/HV devices outperform the SiC limit, revealing the good promise of both vertical GaN and multi-channel lateral GaN devices for MV and HV power applications. Meanwhile, it should be noted that switching tests are required to evaluate the true application space of these GaN devices in comparison with the SiC counterparts, while these tests are still relatively lacking for MV/HV GaN devices. Looking forward, numerous research opportunities exist in physics, materials, and devices for developing 10-20 kV GaN devices, particularly the HV E-mode transistors, for grid applications, as well as the packaging and circuit applications of MV/HV GaN devices.

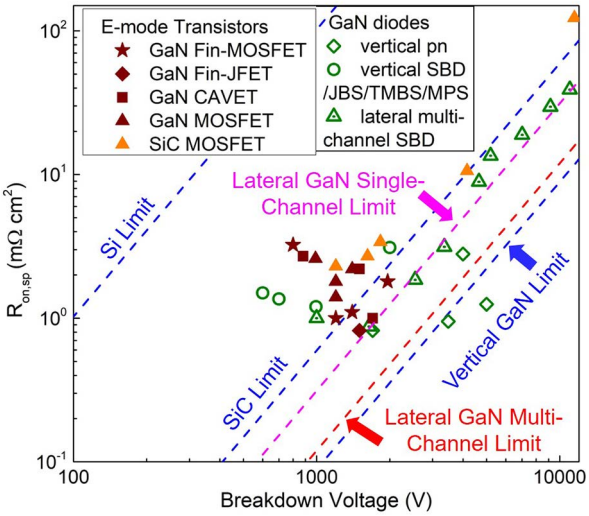

FIG. 7: Specific R_{ON} v.s. BV performance of the state-of-the-art MV/HV vertical and lateral GaN diodes and transistors. The performance limits of 1-D unipolar Si devices, SiC devices, lateral single-channel and multi-channel GaN devices, and vertical GaN devices are also included.

C. Ultra-Low-Voltage Power Devices: Room for GaN?

While extensive efforts are pushing GaN devices towards kilovolt applications, enormous opportunities also exist in the ultra-low-voltage (ULV) end, which are sometimes largely overlooked in the GaN device community. For example, data centers are estimated to consume 10% of the global electric power, and in their power distribution systems, 48 V-to-1 V voltage regulator (VR) modules are placed in the close vicinity to CPUs and GPUs.[73] This 48 V rack architecture has been recently adopted by Google.[73] A two-stage approach is often used in the 48-V VR modules with an intermediate voltage bus of 12 V or 6 V.[73,74] In smartphones and wearable devices, VR modules work at even lower voltages to convert the battery voltage (3.2-4.5 V) to 1 V. The second stage of the 48 V datacenter racks and the VR modules for mobile devices all require ULV 5-30 V power devices that can switch at very high frequency.[75] This frequency upscaling is the key to miniaturizing the VR module and enabling its 3-D integration with processors, i.e., an integrated VR (IVR), which could bring

revolutionary advancements in system efficiency, form factor, and functionality.[75–78]

While Si planar double-diffused MOSFET (LDMOS) is the dominant player in these VR modules, GaN HEMT is uniquely positioned to be a game changer, as it enables much higher switching frequency and the bidirectional conduction. Currently, the lowest-voltage commercial GaN power device is a 15 V, 3.4 A HEMT (EPC 2040), which exhibits 30-fold smaller input capacitance (C_{ISS}), 2.5-fold smaller output capacitance (C_{OSS}), and 30-fold smaller gate charge (Q_G) as compared to a similarly-rated Si LDMOS (e.g., RAL035P01). Very recently, these 15 V GaN HEMTs enabled a smartphone IVR up to 20 MHz,[79] which is 3-10-fold higher than the frequency of Si-based smartphone VRs. These results showcase a good promise of ULV GaN HEMTs, which is further consolidated by the feasibility of monolithically integrating GaN power HEMTs with Si CMOS ICs as recently demonstrated by Intel on 300 mm Si wafers.[80]

However, commercial ULV GaN devices based on the SP-HEMT structure (see Fig. 2(a)) may not be able to exploit the full potential of GaN, particularly for the devices designed for even lower voltages (e.g., sub-10 V). The key design target of ULV HEMTs is to minimize the specific R_{ON}, which is generally proportional to die size, capacitances and charges for a certain current rating, while maintaining the E-mode operation. Different from higher-voltage devices, the R_{ON} of ULV HEMTs is largely contributed by the channel resistance in the gate region (Fig. 8(a)). Note that the channel electron concentration under the gate is determined by gate capacitance (C_G) and gate overdrive instead of 2DEG concentration. In the SP-HEMT, a thick p-GaN, which is needed to realize the E-mode operation, separates the gate far away from 2DEG, leading to a small C_G and transconductance (g_m). The GaN MOS-HEMT with complete gate recess is not suitable for ULV HEMTs as well, as the 2DEG channel is replaced by a MOS channel, which would significantly degrade the channel mobility (μ_{CH}).

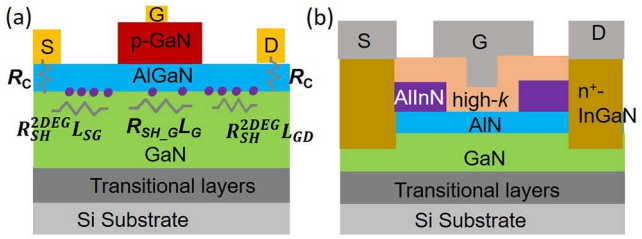

FIG. 8: (a) Illustration of the R_{ON} components and channel electron concentrations in a ULV p-gate HEMT. (b) Schematic of Intel's ULV MOS-HEMT with a partial barrier recess (i.e., AlInN recess under the gate).

Recently, Intel reported a AlInN/AlN/GaN ULV MOS-HEMT that employs a partial barrier recess (removal of AlInN polarization layer) to realize the E-mode operation and uses a composite high-k gate dielectric (effective oxide thickness of 2.3 nm) to produce large C_G and g_m (Fig. 8(b)).[81–83] These ULV GaN HEMTs show over 3.6-fold lower specific R_{ON} as compared to Si LDMOS at 10-20 V, being attractive for both power electronics and RF amplifier applications. Despite the excellent performance, the device fabrication could be challenging, particularly the etch stop at the AlInN/AlN interface retaining the AlN/GaN 2DEG channel. Wafer-level etch uniformity could be a challenge for the large-diameter wafer processing.

FinFETs and trigate HEMTs are other candidates for ULV GaN power devices, as they obviate the delicate partial barrier recess. A thorough review of GaN FinFETs and trigate devices was published recently.[11] These fin-based gate structures realize the E-mode operation via the enhanced 2DEG depletion by sidewall gates and the reduced 2DEG density due to partial strain relaxation. Based on the gate stack, there are three types of trigate HEMTs, comprising Schottky contact, MIS structure, and p-n junction wrapping around the 2DEG fins in the gate region.[11] The schematics of tri-gate GaN MISHEMTs and tri-gate GaN junction HEMTs (JHEMTs)[84] are shown in Fig. 9(a) and (b). These tri-gate HEMTs are initially developed for high-voltage applications. Nevertheless, it has been made explicit very recently that they could allow for a low channel resistance in the gate region and thus suitable for ULV devices.[84] The tri-gate retains the 2DEG channel and places gate metal close to the 2DEG channel, realizing high μ_{CH}, g_m, and C_G concurrently. Ma et al. extracted the averaged sheet resistance in the gate region ($R_{\mathrm{SH\_G}}$) for experimental devices with different E-mode technologies and found a generally 5 to 10-fold lower $R_{\mathrm{SH\_G}}$ in E-mode trigate HEMTs as compared to SP-HEMTs or the MOS-HEMTs with full barrier recess.[84]

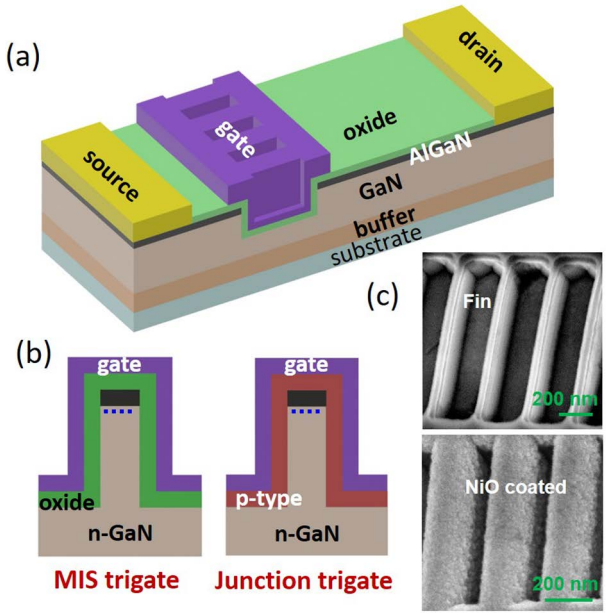

FIG. 9: (a) 3-D schematic of a tri-gate GaN HEMTs and (b) cross-sectional schematic of a MIS-type tri-gate and a junction-type tri-gate. (c) Scanning electron microscopy (SEM) images of the NiO-wrapped AlGaN/GaN fins in a junction tri-gate.

It should be noted that the tri-gate JHEMT is a new tri-gate device that differs from all prior trigate HEMTs.[84] Owing to the higher built-in potential and the obviation of voltage drop in the insulator, the p-n junction can potentially provide a stronger depletion as compared to the MIS stack, making it easier to realize the E-mode operation and suppress short-channel effects. Additionally, the junction tri-gate can minimize the interface trapping and instability issues that are widely reported in the MIS stack. The first tri-gate JHEMT was demonstrated by using p-NiO wrapping around AlGaN/GaN fins (Fig. 9(c)),[84] showing superior performance over the tri-gate MIS-HEMT fabricated on the same wafer.

Despite a decade development of trigate GaN HEMTs, there still lacks experimental demonstrations of their switching characteristics in power converters. This is becoming an immediate need for trigate GaN HEMTs as some other GaN devices are commercially available. Recently, Ma et al. systematically analyzed the static and switching performance space of trigate GaN HEMTs.[85] It was found that the trigate GaN MISHEMT is difficult to provide a superior switching figure-of-merit (FOM), as the benefit from the smaller R_{ON} is compensated by the higher parasitic capacitance in the gate region. In comparison, simulations predict that trigate GaN JHEMTs allow for a much smaller gate capacitance, at the same time retaining the benefits of trigate devices, thereby realizing significantly superior switching FOMs (e.g., the product of R_{ON} and gate/output charges) as compared to planar p-gate GaN HEMTs.[85]

As a summary of Section II.C, the recent availability of 15 V commercial SP-HEMTs have showcased good prospects for using GaN in ULV power electronics. However, the ULV HEMT design, particularly the gate structure design, necessitates very different considerations compared to the higher-voltage counterparts. The MOS-HEMTs with partial barrier recess, FinFETs, and tri-gate HEMTs have shown superior performance over SP-HEMTs for ULV applications. However, many knowledge gaps still exist in their designs, such as the optimal E-mode gate stack and channel materials, and their circuit-level characterizations, particularly the ULV HEMT modules (e.g., a half-bridge module) with integrated GaN drivers. It should be noted that the switching characterization of ULV, high-frequency devices requires a co-optimization with gate drivers and device/module packaging.

D. GaN Devices in Switching: A Unique Platform for Studying Dynamic Device Physics

While many novel devices are showcased in the prior two sections, exciting research opportunities are also present for commercial GaN HEMTs, particularly on their dynamic characteristics in circuit operations. In comparison with Si and SiC power MOSFETs, the complexity of GaN HEMTs comes from not only the fundamentally distinct device physics (e.g., the lack of p-n junctions between source and drain) but also the heterogenous GaN-on-Si epitaxy with a high dislocation density. Many issues regarding device stability, reliability, and robustness arise from the presence of traps in various regions of the epi structure. The occupation probability of these traps depends on the electrical history, e.g., device switching locus and bias history. Trapping behavior (trapping and detrapping) are usually time-dependent with time constants that can span many orders of magnitude.[86] Hence, device characteristics in fast switching could significantly differ from the ones under DC conditions. GaN HEMTs have become a unique platform for studying device physics under nonequilibrium conditions, e.g., the concurrent presence of high electric field, fast switching, and high temperatures. Numerous reviews have periodically summarized progress in GaN reliability studies,[86–90] and a recent paper nicely overviews the relevant device physics and material issues.[86] After several GaN HEMTs having passed reliability qualifications are commercially available, many recent studies emphasized on testing them in switching circuits and mission profiles as well as understanding their robustness outside the safe-operating-areas and close to device destruction limits. Here, we attempt to take a snapshot of some interesting findings in these endeavors. Some of the application-oriented device issues and their relevance to the internal trapping behavior is illustrated in Fig. 10.

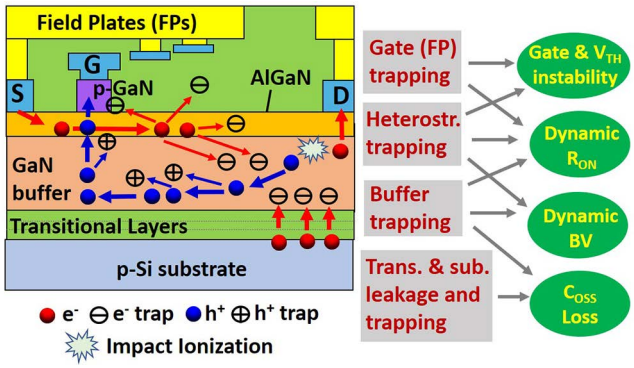

FIG. 10: Schematic of the electron/hole dynamics and trapping inside a p-gate HEMT during high-voltage power switching, with the illustration of different trapping mechanisms and their correlation with several device phenomena.

Dynamic R_{ON} phenomenon, where R_{ON} immediately after device turn-on is higher than the DC value, is a well-known issue of GaN HEMTs that increases their conduction losses in power converters. A decade of study has revealed its origins to be associated with buffer trapping, surface trapping and gate instability.[91] However, a large variation of dynamic R_{ON} has been reported in the literature, spanning from a minimal increase over static R_{ON} to ten times higher, even for commercial devices. It was recently pointed out that this inconsistency largely originates from characterization methods.[92] The standardized double-pulse-test method, which does not specify the voltage-blocking time and ignore the accumulation effects in repetitive switching cycles, could significantly overestimate the device dynamic R_{ON} in power converters. The on-wafer pulse I-V measurements cannot mimic the switching locus

and slew rate (e.g., dv/dt) in real converter applications. Instead, steady-state switching measurements are essential for prediction of in situ dynamic R_{ON}.[92] The worst-case dynamic R_{ON} of commercial GaN HEMTs measured in this framework was found to be less than 2 times higher than the static value. Additionally, the dynamic R_{ON} differs in hard switching and soft switching is often impacted by hot-electron effects in hard switching.[93–95] Very recently, dynamic R_{ON} of commercial GaN HEMTs was measured in multi-MHz soft switching and shows a saturation at ∼2 MHz, a frequency exceeding the relevant trapping and detrapping time constants.[96]

The BV of commercial GaN HEMTs was also found to be dynamic and, interestingly, higher than the static BV measured in quasi-static I-V sweeps.[97,98] The dynamic BV of commercial devices were measured in a unclamped inductive switching (UIS) setup with the UIS pulse widths that span eight orders of magnitude (25 ns to 2 s), showing a decrease with prolonged pulse width (Fig. 11).[97] The dynamic BV of a 650-V rated SP-HEMT was found to exceed 1400 V in 25 ns pulses, about 450 V higher than the static BV. This higher dynamic BV is attributed to the reduced buffer trapping in short pulses, where the buffer trapping intensifies the peak electric field near the drain side and makes it reach the critical electric field of GaN at lower drain biases.[97] To understand the overvoltage margin in continuous switching, this commercial HEMT was subsequently measured in repetitive hard switching cycles with a overvoltage of 1330 V (over 90% dynamic BV), and it showed small and recoverable parametric shifts after 1 million cycles.[98] The parametric shifts were found to be induced by the trapping of the holes produced in impact ionization during overvoltage events.[98] These results suggest the dynamic BV provides GaN HEMTs an additional overvoltage margin in power converters. Interestingly, while electron trapping governs the dynamic BV (i.e., the failure boundary), hole trapping dominates the device parametric shifts under repetitive overvoltage stresses.

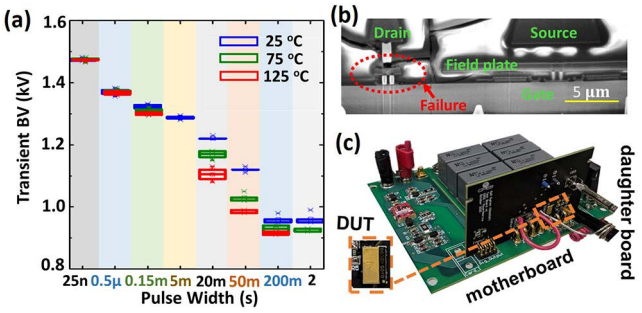

FIG. 11: (a) Box plots of the dynamic BV of SP-HEMTs failed at different pulse widths and temperatures. (b) Cross-sectional SEM image of the device failed in 25 ns pulse, showing the failure location at the drain side. (c) Photo of the test setup with a motherboard/daughter-board configuration. Reproduced with permission from IEEE International Electron Devices Meeting 23.3 (2020) and IEEE Electron Device Lett. 42, 505 (2021). Copyright 2020 and 2021 IEEE.

The above breakdown mechanism of GaN HEMT is fundamentally different from that in Si/SiC MOSFETs, which is usually governed by avalanche and shows minimal time dependence. The lack of avalanche capability makes GaN HEMTs withstand the surge energy in power converters in a very different way, where the surge-energy withstand capability is crucial in EV powertrain and power grid applications.[99–101] The GaN HEMTs were found to be not able to dissipate the surge energy through avalanching, but instead, withstand it through capacitive charging. The maximum surge energy that it can withstand is determined by the output capacitance (C_{OSS}) and dynamic BV;[99,100] the failure is electric field induced rather than thermally limited as in the avalanche. This capacitance-related ruggedness suggests a fundamental trade-off between the HEMT's surge-energy ruggedness and its switching speed and losses. It should be also noted that the absence of avalanche capability is not due to GaN but the HEMT structure; robust avalanche has been demonstrated in vertical GaN p-n diodes and Fin-JFETs.[30,31,40,41]

Another interesting finding of GaN HEMTs in power switching is the C_{OSS} losses, i.e., the losses from charging and discharging the device C_{OSS}, which is assumed lossless for ideal power switches.[102–105] These losses are of particular importance in soft-switched circuited at MHz switching frequencies. This unexpected loss mechanism was first found to be a universal phenomenon for different commercial GaN devices regardless of device packaging.[102] Later, it was found that this loss is related to buffer region, and an enhanced multi-layer nitride buffer allows a significant loss reduction.[103] Similar C_{OSS} loss was also reported in SiC devices,[104,106] and a circuit model was developed to describe its bias- and frequency-dependence.[105] A very recent investigation speculates that the C_{OSS} losses include both resistive losses due to the resistance of buffer layers and Si-substrate and the capacitive hysteresis loss due to trapping dynamics.[107]

Finally, SP-HEMTs and GITs usually have a relatively small gate voltage (V_G) operation margin; this motivates the active investigations of gate reliability[108] and the associated dynamic threshold voltage (V_{TH}) issue.[109–112] The dynamic V_{TH} was found to originate from the charge storage in p-GaN during switching,[111] and thereby depends on the p-gate contact, e.g., Schottky- or Ohmic-type.[109] The Ohmic-type p-gate generally shows smaller dynamic V_{TH} due to a superior capability of charge supply and extraction. A similar trade-off is also present in the buffer trapping, where the hybrid drain (i.e., p-GaN connected drain[113]) can inject holes to suppress the buffer trapping and thus alleviate the dynamic off-state current[114] and dynamic BV[97] issues.

E. Superjunction: The Next GaN power device?

Upon reflection, despite the existence of some simulation designs,[115] p-n junctions have never been used in commercial GaN HEMTs for enhancing the electric field management and BV ruggedness. The recent device results, such as the new capabilities demonstrated in Fin-JFETs and tri-gate junction HEMTs, seem to imply vast benefits of using p-n junctions

and 3-D channel structures (e.g., fins) in future GaN power devices. One of the most successful power devices in Si that employ junctions is the superjunction, which relies on alternative n- and p-doped pillars and can break the theoretical trade-off between R_{ON} and BV of 1-D drift regions.[116] The superjunction was recently realized in SiC[117–119] but have not reached experimental demonstrations in GaN. Instead of p-n junction, a balance in polarization charges, i.e., "polarization junction", was used in lateral AlGaN/GaN devices to produce a "natural superjunction" for superior electric field management.[120–122] The natural polarization based power converter has also been reported,[123] and the safe-operating-area of these devices have been studied.[124] Despite the demonstration and application of these devices, their R_{ON} is still much higher than the 1-D GaN limit (and even the SiC limit).

The recent experimental realization of selective p-type doping in GaN power devices[35,40,41,50] has removed some critical roadblocks for fabrication of GaN superjunction devices. In addition to selective p-n junctions, selective p-GaN/2DEG junctions with a high blocking electric field have also been demonstrated.[125] Simulations predict that vertical GaN superjunction transistors with fin channels and 2DEG channels can enable at least 20-fold smaller capacitances and charges compared to today's best MV transistors and allow multi-MHz, multi-kilovolts power switching up to 10 kV.[126] An analytical model to design a superjunction with interfacial charges,[127] which were usually present in selective p-n junctions,[128] was also reported. Given these progresses, we believe the GaN superjunction exceeding the 1-D GaN performance limit will arrive soon. To accelerate their development, vast material- and processing-level efforts are required to address a few issues in GaN, such as the selective-area p-type doping, incomplete acceptor ionization and the resulted difficulties in charge match, leakage current control, acceptor activation in deeply buried structures, etc.

Meanwhile, novel lateral GaN superjunction HEMTs that combine the 2DEG channel and the superjunction functionality can be also envisioned. While the existing polarization superjunction devices show a much larger R_{ON} compared to the GaN superjunction limit, the employment of multi-channel structures can potentially lower the R_{ON}. Many relevant designs have been proposed[129–132]. In particular, the recent 10-kV multi-channel RESURF SBD, a "quasi-" multi-channel polarization superjunction, breaks the SiC limit and show the promise of multi-channel polarization device[23]. The other option is to selectively introduce p-GaN regions into the 2DEG channel building on the recently demonstrated p-GaN/2DEG junction for electric field management.[125] Finally, the incorporation of heterogeneous p-n junction like the p-diamond/n-GaN junction[115,133] into the HEMT structure has also been proposed, and the heterogeneous superjunction could also be envisioned. Experimental explorations of these new device concepts may bring new capabilities and great advancements in lateral GaN HEMTs.

III. GAN FOR RF ELECTRONICS

A. RF Circuits and Applications

Compared with GaAs, Si, and SiGe, GaN technology offers ideal material characteristics for RF power applications such as satellite communication and 5G cellular communication. As shown in Fig. 12, thanks to GaN's higher power density in the frequency range of 2–7 GHz (FR1 band) and millimeter wave bands ($>$ 24 GHz, FR2 band), GaN dominates RF power applications. For the 5th generation (5G) and beyond wireless communication, wider signal modulation bandwidths ($> 100-400$ MHz) are needed for base station transmitters. A similar trend is observed for Ku- and Ka-band satellite communication. PA is the most power-hungry part of the high-power radio transmitter, and thus improving its efficiency has always been a major research focus and is also one of the topics of discussion in this section. Advanced energy-efficient PA architectures (e.g., Doherty amplifiers), combined with the cutting-edge GaN HEMT devices, have shown outstanding performance in recent works.[134] Figure 13 illustrates the impact of GaN device characteristics on the PA metrics and system-level advantages such as smaller footprint and reduced total cost of ownership (equipment capital, energy and thermal management expenses,) for the operators. It is important to note that the RF transmitter compactness and thermal handling are some of the key system-level requirements of 5G massive multiple-input multiple-output (MIMO) and small cell base stations, where many compact RF front-end modules, including PAs (e.g., 64 or 256 antenna elements half-wavelength spaced panel), are installed as active antennas for beamforming purposes in both urban and sub-urban areas. GaN PA technology manifests itself as a well-suited solution here.

Among several emerging wideband GaN PA technologies including continuum-mode (i.e., class-J), outphasing, envelope tracking (ET), and advanced Doherty, here we highlight two promising techniques: ultra-high speed switching mode and artificial intelligence (AI)-assisted RF PA. These two PA architectures, combined with the aforementioned GaN device merits, show great potential of efficient amplification for wideband radio signals used in the next-generation radio transmission, in which dynamic spectrum allocation/sharing and radio traffic are significant considerations.

Higher power efficiency, while maintaining the required linearity specifications, is the main driver of RF PA advancement for cellular applications as shown in Fig. 14. There have been various PA architectures proposed for different generations of mobile communications. Conventional Doherty PAs using LDMOS and GaN (in recent years) have been the workhorse for the infrastructure of transmitters, thanks to their relatively simple implementation (i.e., analog power dividers and combiner) and competitive power efficiency of 30-40%. Numerous innovations are taking place related to the design of next-generation RF PAs, such as the ET PA and digitally assisted Doherty amplifiers, where GaN HEMTs have been adopted due to their much faster and lower loss switching properties, which are key for RF switching-based circuit de-

FIG. 12: Current RF power device technologies for high frequency applications. Reproduced with permission from IEEE/MTT-S International Microwave Symposium Proceeding. Copyright 2020 IEEE.

FIG. 13: GaN HEMT device physical characteristics offer circuit and system benefits for RF applications. Reproduced with permission from IEEE Microwave Magazine. Copyright 2017 IEEE.

signs. Studies have been reported for both wireless and radar applications using GaN ET circuit designs with promising results at increasingly wider instantaneous signal modulation bandwidths ($20-80$ MHz) and higher operating frequencies.

A 5 W chip (size of 1×2.4 mm^2) in 0.15 μm GaN HEMT process was reported for an advanced soft-switching ET modulator, also named as a switching buck converter (SWBC). Soft switching employs a diode and an inductor that resonates with output capacitance of the GaN FETs at the switching frequency, as shown in Fig. 15(a). Soft switching minimizes the overall power loss, which is proportional to the switching frequency and is thus an enabler for efficient amplification at higher switching frequencies for future wider band modulated signals. Low parasitics are strongly desired and required, and challenging to achieve with Si-LDMOS at switching frequencies over 10 MHz. Figure 15(b) shows the switching frequency dependence of the Soft-SWBC and hard-switching BC (Hard-SWBC). At 200 MHz switching frequency, the measured Soft-SWBC efficiency was 77% for 6.5 dB PAPR (peak to average power ratio) with 20 MHz modulation signal. Even with high switching frequency of 450 MHz, it still maintained 67% total efficiency ($>$ 20% higher efficiency compared with Hard-SWBC). The overall RF PA efficiency including ET converter was more than 47% at 3.6 GHz[135]. In 2020, FBH reported a 0.25 μm gate length GaN HEMT-based design of envelope modulator supporting 300 MHz modulation bandwidth.[136] Over 60% efficiency is demonstrated for ultra-wideband modulated signal applications. One of the practical challenges for GaN switching applications is the design of the gate driver stages to properly turn ON and OFF the final stage with high speed and efficiency. This has been one of the bottlenecks for GaN switching applications. In the work by Hühn *et al.*,[136] a hybrid module implemented with a pre-amplifier MMIC, a switching mode driver stage MMIC, and a charge pump with discrete elements, reached 900 MHz switching frequency.

FIG. 14: From Analog to Digital: Advanced RF PA roadmap for sub-6 GHz (FR1). Reproduced with permission from IEEE Microwave Magazine. Copyright 2017 IEEE.

GaN Doherty amplifiers have shown promising performance at mm-Wave bands.[137] In recent work, a GaN Doherty chip of size 2.7×1.6 mm^2 achieved peak power added efficiency (PAE) of 23%, 8 dB back-off PAE of 15% over the frequency of 27.5 to 29.5 GHz. The back-off PAE with over 3 W output power is one of the highest for Ka-band (frequency $>$ 27 GHz) MMIC amplifiers. Figure 16 shows MMIC GaN Doherty chip and the measured output power spectrum under 64QAM 100 MHz modulated signal at a carrier frequency of 28.5 GHz before applying digital predistortion techniques. In summary, these studies showed that advanced PAs designed with cutting-edge GaN HEMTs are powerful solutions for both sub-6 GHz and mm-Wave bands.

B. Hardware-Software Co-design

To fully unlock the GaN device potential in RF applications, innovations at all levels including device process ad-

FIG. 15: (a) A GaN soft-switching circuit. (b) Performance comparison versus switching frequency of soft- and hard-switching buck converters.[135] Reproduced with permission from IEEE/MTT-S International Microwave Symposium Proceeding. Copyright 2018 IEEE.

FIG. 16: (a) 28 GHz GaN Doherty amplifier and (b) its measured output power spectrum.[137] Reproduced with permission from EEE/MTT-S International Microwave Symposium Proceeding. Copyright 2020 IEEE.

vancement and circuit architecture enhancement and modifications are necessary. In particular, the recent trend of software-hardware co-design with machine learning techniques has demonstrated exciting opportunities.[138,139]

As shown in Figure 17(a), a revised version of Doherty amplifier was introduced by modifying the analog input into to two separately controllable RF inputs, which are then optimized by the artificial intelligence (AI) algorithm on the fly, depending on the real-time dynamic operating conditions, such as frequency and input power levels. As a result in Figure 17(b), a mixed mode high-efficient RF PA was first demonstrated to operate over an ultra-wide bandwidth covering $1.4-4.8$ GHz with over 45% efficiency. Results show that the AI engine can optimize GaN HEMT bias conditions, the dual-input signal phase, and amplitude for achieving superior performance.

The AI engine can be designed and implemented using the silicon CMOS technology. Therefore, a heterogenous integration of CMOS and GaN technologies, leveraging the unique advantages of silicon and III-V compound semiconductor technology, is one of the enabling technologies to achieve the best trade-off between performance and cost at the system level. Some initial work has been reported, as shown in Figure 18, in which CMOS and GaN are integrated by bonding two separate chips. It achieved output power in the range of 2-3 W and drain efficiency of over 50% spanning more than an octave of bandwidth.[140] This digitally assisted technique allows the digital power DAC approach to be extended to higher power levels and bandwidths than previously demonstrated. Such features are exciting and attractive for the realization of future software-defined radio, cognitive radio, where the performance of the digital, AI, and other technologies are co-designed and co-optimized.

C. Device Architectures for RF

As discussed previously, III-N semiconductors exhibit significant potential for RF applications, thanks to the combination of wide bandgap ($\sim$ 3.4 eV), high electron saturation velocity (2×10^7 cm/s), and high electron mobility ($\sim$ 2000 cm^2/V·s). From the initial days in AlGaN/GaN HEMT research, its RF potential has been noted given its superior performance when compared with other wide bandgap semiconductors.[141] Since then, the f_T of deeply scaled GaN transistors has reached $>$ 450 GHz for GaN-on-SiC transistors and $>$ 300 GHz for GaN-on-Si transistors.[142–144] The improvement in the cutoff frequency was driven due to a combination of high channel mobility, superior carrier confinement (reduced short-channel effects due to back barrier), T-shaped/mushroom gates with short gate foot ($L_G < 80$ nm) and large gate head), small access region lengths (possibly self-aligned process), good ohmic contacts (contact resistance

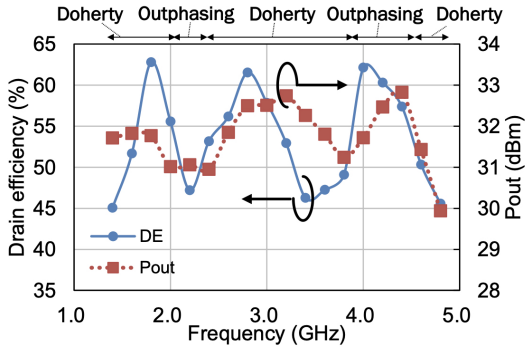

FIG. 17: (a) Machine learning assisted dual-input mixed-mode GaN PA. (b) its measured performance over ultra-wide bandwidth.[138,139] Reproduced with permission from EEE/MTT-S International Microwave Symposium Proceeding. Copyright 2019 IEEE.

FIG. 18: A digitally controlled CMOS/GaN PA[140]. Reproduced with permission from IEEE Radio Frequency Integrated Circuits Symposium Proceedings. Copyright 2016 IEEE.

$<$ 0.2 Ω·mm, using regrown n^+ contacts), reduced trapping (e.g., via improvement in the surface passivation technology). Future improvements in the cut-off frequencies, possibly up to the 700 GHz range, would depend on improvements in the epitaxial structure (lower sheet resistance, thinner barriers, superior carrier confinement), as well as the overall device structure. Evidently, this is no easy feat considering existing challenges. In terms of material properties, the sheet resistance of the channel would need to be reduced to $<$ 150 Ω/sq by increasing the carrier density while maintaining high carrier mobility. Short-channel effects need to be significantly suppressed, for example, through the use of thin Schottky barrier (pure AlN as opposed to AlGaN),[145] back barrier,[145–147] tri-gates.[148] These modifications add complexity to the conventional AlGaN/GaN device. In terms of fabrication, reliable ways to achieve gate metallization (typically T-shaped/mushroom gates with small gate foot and large gate head) are highly desired.[149]

GaN HEMTs have been the workhorse of PAs in the Ka band and beyond. For example, in as early as 2005, an AlGaN/GaN HEMT showed performance of 10.5 W/mm at 33 % power-added efficiency (rail voltage of 40 V) at 40 GHz.[150] While traditional AlGaN/GaN HEMTs have been commercialized for RF applications, research into technologies for the next generation of GaN transistors could be mainly grouped into two categories, namely epitaxial structure and device innovations. In terms of epitaxial structure, structures like ScAlN/GaN, AlN/GaN, N-polar GaN/AlGaN, InAlGaN, and multi-channel $(AlGaN/GaN)_n$ have been proposed.[151–156] In Ga-polar AlGaN/GaN HEMT the electron density in the channel can be enhanced by increasing the barrier (AlGaN) thickness which is essential to improve the power density of RF devices. However, a thick barrier reduces the gate capacitance hence leads to poor gate control as well as low-transconductance. One major benefit of N-polar GaN-HEMT devices is that it decouples these two parameters: 2-DEG density and barrier thickness making it possible to achieve higher power density at higher frequency compared to a Ga-polar lateral device. Additionally, in N-polar devices, when an AlGaN layer is placed on top of the GaN channel, the polarization field opposes the electric field produced in a reverse-biased gate drain junction. This is in contrast to Ga-polar HEMTs where the polarization field is in the same direction and an applied gate-drain reverse bias rapidly reduces the tunneling barrier for gate-injected electrons. All these benefits coupled with atomically deposited Ru gate technology leads to the record breaking performance in terms of power density (6.2 W/mm) and power added efficiency (33.8%) at 94 GHz.[149] Another material-innovation is the use of ScAlN as a barrier layer in GaN HEMT devices. Because of the higher spontaneous polarization coefficient of ScAlN, ScAlN/GaN can be lattice-matched with up to 2$\times$ sheet charge density compared to $In_{0.18}Al_{0.72}N$/GaN.[157] A lattice-matched Sc-based barrier enables high sheet charge density without strain and may enhance reliability and thin barrier leads to better RF performance.

Unique operation principle of GaN-based field effect transistors with laterally-gated multiple 2-DEG channels, called

BRIDGE FETs (buried dual gate FETs) demonstrated device characteristics suitable for efficient and linear millimeter-wave power amplifier applications. In these devices, parallel gates buried into an Al(Ga)N/GaN HEMT epitaxial structure form lateral Schottky contacts to the 2DEG channel layer.[158] An absence of the top gate contact makes the device unique in contrast to conventional transistors in its operation principle; the drain current is controlled solely by modulating the width of the 2DEG while maintaining its sheet electron density. The benefits of Bridge FET include: (a) negligible current collapse, (b) low output conductance due to improved electrostatics, (c) highly uniform capacitance, and (d) low gm3 compared to T-gate HEMT.

To achieve even higher power output for 5G base stations etc., fundamental innovations are necessary in the device structure, beyond the current lateral structure (carriers move horizontally in the channel), possibly by drawing valuable lessons from the development of vertical power transistors. These vertical structures offer several benefits including high breakdown voltage (determined by the thickness of the drift region), high power density per unit chip area (due to bulk conduction in the vertical direction), more uniform thermal dissipation (due to the bulk conduction), and possibly better reliability (due to buried channel without the presence of surface states). Early studies on the RF characteristics of vertical devices have been conducted demonstrating their suitability for RF application.[159,160] Recent experimentally calibrated simulations of a proof-of-concept single-fin vertical FinFET have predicted output power of > 15 W/mm in the Ka band.[161] Actual vertical FinFETs typically feature large-area arrays, which can significantly increase the power output of the device.[162] While initial results are promising, further research is required to address materials and fabrication challenges to realize this innovative device structure.[20]

1. RF linearity

To meet the stringent requirements of mm-Wave communications in 5G and beyond, linearity is equally important as achieving high power amplification at high frequencies. The presence of non-linearity often forces the circuit to operate at back-off output levels, at the expense of lower efficiency. The origins of non-linearity at the device-level include the g_m degradation under high currents, gate capacitance non-linearity, and memory effects due to carrier trapping.

While circuit-/system-level compensation techniques (e.g. digital pre-distortion (DPD) and Doherty amplifier topology) have been widely used to improve efficiency and reduce non-linearity, they bring additional complexity to the circuitry. Furthermore, in the 5G MIMO era, DPD techniques are limited by the bandwidth, especially for ultra-broadband PAs. Therefore, significant attention has been paid to the device-level solutions that can inherently offer higher linearity.

In terms of the epitaxial structure, research has focused on the modification of the conventional AlGaN/GaN heterostructures. An early work proved that the AlGaN barrier thickness impacts the device linearity.[163] Moreover, the concept of graded channel (colloquially, "three-dimensional electron gas, 3DEG") has been proposed to improve linearity, as demonstrated in the AlGaN channel polarization-graded field-effect transistor (PolFET) [164] Improvements in device fabrication, e.g., the use of different passivation layers, have further improved the linearity and DC-RF dispersion of PolFETs.[12,165] The second type of innovation to the epitaxial structure is the use of multi-channel heterostructures. Early works on planar gate devices have demonstrated higher linearity, which at the device-level, is reflected in the broader g_m peak.[166,167]

Advancements in GaN device technology, notably the FinFET, have opened up the design space in the third dimension (previously parallel to the gate width), therefore offering new device possibilities for higher linearity.[168,169] It is evident that FinFETs have made the electrostatic control of the multi-channels more effective by exerting lateral (sidewall) control over the bottom channels. A linearity figure-of-merit of OIP_3/P_{DC} of 6 dB at 30 GHz has been reported on the SLCFET.[155] The use of laterally gated structures and sloped gate recess have been reported to address the linearity issues of GaN devices.[170,171]

FinFETs allow for the combination of many different types of fins (each giving different threshold voltage, V_{TH}) in the same device (that shares the three transistor terminals), thus allowing for flexibility in the fin distribution for linearity.[172] Similar concepts have been used for laterally gated devices and an improved distribution of fins.[173–178]

A fundamental innovation that could potentially simultaneously deliver higher linearity and RF efficiency is the GaN CMOS technology. Circuit topologies based on CMOS, as opposed to single-type logic, have proven to be beneficial for linearity.[14] Furthermore, the use of p-FETs as loads could provide high output resistance at the output node, while conserving the much-needed chip area (as opposed to using inductors).

2. Other consideration for RF

In high-power RF applications, the device is constantly biased near or even beyond the power compression point for high efficiency. At such a high power output level, self-heating is a major concern. Prolonged self-heating in the junction, in particular the non-uniform self-heating in the narrow regions near the AlGaN/GaN interface, often exacerbates the concerns of device reliability. To address the self-heating in GaN HEMTs, two approaches are being explored. The traditional approach relies on the use of high thermal conductivity substrates (e.g., diamond), surface passivation, and packaging, and several GaN-on-diamond HEMTs with good performance have been reported.[179–181] The second approach, a more challenging but possibly more rewarding one, is the use of vertical device structures, which has been proposed to give more uniform thermal distribution and lower peak junction temperatures when compared to lateral HEMTs.[161]

While GaN electronics scalable up to 300 mm wafers have been demonstrated, their CMOS compatibility has been a concern.[80] In terms of ohmic contact technology, alloyed contacts

have been preferred over MBE regrown contacts. However, alloyed contacts typically contain gold and hinders CMOS compatibility in such front-end-of-line processes. Transistors with a CMOS-compatible metallization process have been demonstrated with good performance of $f_T = 210$ GHz .[182,183] While these developments are encouraging, the trade-offs with CMOS compatibility (e.g., sub-optimal device performance) would need to be weighed against their benefits of fully CMOS-compatible GaN process. The booming market for wide bandgap semiconductors, like GaN, have sustained dedicated foundries for these technologies. Furthermore, the possibility of heterogeneous integration and packaging advancements (e.g., flip-chip) are also important considerations.

IV. GAN FOR DIGITAL ELECTRONICS

III-N alloys have remarkable material properties that could benefit advanced technology nodes with sub-10 nm channel lengths. Wider bandgap of III-N semiconductors, in comparison to Si and other compound semiconductors, leads to significant reduction of band-to-band tunneling and gate-induced drain leakage that in turn reduces the off current and, hence, the static power dissipation. Because of the high optical phonon energy of 93 meV[184] and wide valley separation (nearest valley to Γ is M and it is > 1 eV apart), fully ballistic transport is expected in the sub-10 nm channel length regime.[185,186] This is corroborated by experimental demonstration of room-temperature ballistic transport in InAlN/GaN heterostructure-based 2DEG. Having a GaN-based advanced logic platform opens up a plethora of opportunities such as GaN-based on-chip optical interconnects, thanks to the maturity of GaN-based photonic and optoelectronic devices,[187] steep subthreshold devices using the peizoelectricity and polarization charge properties,[188,189] and a fully integrated MEMS platform based on AlN. Apart from these, spontaneous and piezoelectric polarization in III-Ns offer a new degree of freedom to dope the source and drain regions without the impact of Random Dopant Fluctuation (RDF) effects and thermal diffusion of dopants.[190,191] All these benefits make GaN-based channels an intriguing option for advanced technology nodes, which could complement the well-established markets of GaN for RF, power electronics, and optoelectronics.[192]

The first extensive study that explores the potential of GaN channel for advanced nodes identifies two key material parameters: (i) effective mass of electrons, m_{eff}, and (ii) relative permittivity of the semiconductor channel, ε_r, that impact the performance of the gate-all-around (GAA) nanowire (NW) transistors with ultra-scaled square cross-section.[193,194] This work identifies a range of $m_{\text{eff}} \in [0.3, 0.4]m_0$ that minimizes the tunneling probability ($T \propto \exp\left(-\sqrt{m_{\text{eff}}}\right)$ and thus the off-state current, while also achieving a higher on-current (I_{ON}). Likewise, when ε_r is too low (i.e., in the range of 1-5), I_{ON} and g_m are reduced due to the lower gate-to-channel capacitance. However, when $\varepsilon_r > 15$, the device suffers from short-channel effects. Hence, an optimal range of $\varepsilon_r \in [7, 13]$ was identified to achieve the best sub-threshold to above-threshold device performance. Figure 19 summarizes the afore-mentioned findings. Since m_{eff} of GaN NWs with scaled dimensions is around $0.37m_0$[195] and ε_r of GaN is 8.9,[196] GaN satisfies the optimal criteria identified in Ref. 193 and, thus, GaN GAA NW transistors are expected to outperform Si, Ge, InAs GAA NW transistors with similar dimensions.

The influence of the geometric shape of the GaN NW n-FET on its performance for digital logic has been extensively studied.[197] The performance of square, circular, triangular, and hexagonal GaN-NW nFETs are estimated using atomistic nearest-neighbor tight-binding (TB) $sp^3d^5s^*$ basis in NEMO5.[198] It is observed that the circular, triangular, and hexagonal devices all have higher raw current than the square geometry despite their smaller cross-sectional area. The superior performance of circular, triangular and hexagonal cross-sections can be attributed to the relatively larger effective mass of carriers, which suppresses the source drain direct tunneling leakage. First-principles calculations[195] and DMol calculations [199] also show that the effective mass of carriers increases with a decrease in the NW diameter. For the same NW thickness, the triangular structure possesses the highest g_m and the lowest subthreshold swing (SS) among the four geometries; thus, the triangular NW allows for better cross-sectional scaling than the square NW.

Even though the initial device simulation results show promising intrinsic performance in terms of key device parameters like transconductance (g_m), sub-threshold swing (SS) and ON-current density (I_{ON}), when compared with Si nanowire FETs, there are several challenges as discussed next that will need to be overcome before III-N platform can be considered a viable option for future technology nodes.

a. Nanowire etching Scaled GAA transistors require smooth etched surfaces, as surface roughness can cause device-related issues such as mobility degradation and threshold voltage variation. For FinFETs, after etching the fins with BCl_3/Cl_2 based plasma with a Ni-based hard mask, the vertical surfaces are smoothed using hot tetramethylammonium hydroxide (TMAH) treatment. However, this method is unlikely to work for the NWs because of the anisotropic nature of etching. A recently demonstrated digital etch technique using repeated piranha and HCl etch might be a potential solution to this problem in the near future.[200]

b. Lack of high performance p-channel FET Lack of high performance p-FET is another limitation of III-N platform. Logic technology requires both n-FET and p-FET with similar device performances as it significantly reduces static power dissipation. Several factors limit the performance of p-FETs based on III-N semiconductors such as low hole mobility due to the heavy hole mass, limited hole concentration due to the high activation energy of Mg dopants for p-GaN, and higher contact resistance resulting from the unavailability of high workfunction metals.[201]

c. High defect density of GaN-on-Si wafers Commercial viability of a certain semiconductor technology, especially for digital applications, demands the availability of large diameter wafers with very low defect density. High performance GaN n-FETs on 300 mm GaN-on-Si wafer from Intel Corporation demonstrates the scalability of GaN-on-Si technology.[80]

FIG. 19: (a) Impact of effective mass of electron in the channel material on I_{DS}-V_{GS} characteristics; (b) Variation of on-current with the effective mass of electron in the channel material for $V_{CC} = 0.5$ V and $I_{\text{off}} = 1$ nA/μ m; (c) Variation of on-current with the effective mass of electron in the channel material for $V_{CC} = 0.5$ V and $I_{\text{off}} = 100$ nA/μ m; (d) Impact of electron permittivity of the channel material on I_{DS}-V_{GS} characteristics; (e) Variation of on-current with the electron permittivity of the channel material for $V_{CC} = 0.5$V and $I_{\text{off}} = 1$ nA/μm; (f) Variation of ON current with the electron permittivity of the channel material for $V_{CC} = 0.5$ V and $I_{\text{OFF}} = 100$ nA/μ m. Reproduced with permission from IEEE Electron Device Lett. 38 (7), 859 (2017). Copyright 2017 IEEE.

However, the defect density of GaN on Si platform is quite high ($\sim 10^9 - 10^{10}$ cm^{-2}) and likely the bottleneck to production yield, which arises from the thermal and lattice mismatch between the crystals of GaN and Si. Engineered substrates could potentially be an option in this case. Recent demonstration of GaN vertical power devices on an engineered substrate have yielded low defect density large diameter wafers up to 200 mm. However, 300 mm GaN on engineered substrate wafers still awaits experimental demonstration.

V. GAN INTEGRATED CIRCUITS

The high critical electric field of GaN, in combination with its excellent transport properties, allow for GaN power transistors with much shorter drift regions and narrower gate widths than their Silicon or SiC counterparts. This allows for significantly lower gate capacitances and faster switching frequencies than traditional power switches at the same operating voltages. To take full advantage of the reduced gate capacitance and high switching speed of GaN power transistors, it is necessary to minimize parasitic inductances between the power switches/transistors and the gate driver circuit. For this, the GaN community has traditionally leveraged enhancement-mode/depletion-mode logic also known as direct coupled logic (DCL) to integrate relatively simple gate-driver circuits on the same chip than the GaN power devices, however this technology suffers from significant power consumption and limited circuit design flexibility. To overcome these issues, recently there has been a lot of research on a new all-GaN complementary technology that allows for the integration of high-performance n-channel and p-channel GaN enhancement-mode transistors on the same chip without the need of epitaxial regrowth or special processing.[192,202–207]

Fig. 20(a) shows the epitaxial structure used for the demonstration of the all-GaN complementary technology. This structure was grown by the company Enkris Semiconductor, Inc. on 6 in. Si wafers. As shown in Fig. 20(b), enhancement-mode (E-mode) *p*-type transistors can be fabricated by contacting the two-dimensional hole gas at the top GaN/AlGaN interface, while *n*-type devices are obtained by recessing the structure to allow direct ohmic contact connection to the two-dimensional electron gas at the bottom AlGaN/GaN interface. A simple gate driver is shown in Fig. 20(e) where a 350 pF load is switched at 100 kHz frequency.

Although the first generation of GaN E-mode p-FET de-

vices shown in Fig. 20(b) had a maximum current density of 10 mA/mm, current densities in excess of 50 mA/mm have been demonstrated by scaling down the gate length.[205] The performance of these E-mode devices can be further improved by reducing the contact resistance and increasing the doping levels in the top p-GaN layer.

GaN p-type transistors, in particular those developed on scalable GaN CMOS platforms, have received significant attention in recent years, not only because of their novelty and high performance, but more importantly, because of the tremendous potential for future GaN CMOS circuits.[192] Even though discrete p-type and n-type transistors were developed early, the integration technology of both of these components remained challenging, particularly in the context of university fabrication facilities. In Ref. 206, the logic inverter behavior was quantified using the MVSG-based modeling of p-FET and n-FET on the regrowth-free GaN complementary logic platform. In the later experimental demonstration of such a logic inverter, the measured DC transfer result was found to closely follow the simulated characteristics.[192] This proves that the model adequately accounts for the key characteristics, such as the threshold voltage, capacitances, parasitic resistances, and relative current levels, of the newly developed p-FET and n-FET devices on the GaN CMOS platform. The GaN CMOS simulation framework was also scaled up to estimate the performance of digital logic building blocks (including 6-T SRAM) at room temperature.[208]

VI. GAN FOR QUANTUM COMPUTING APPLICATIONS

Quantum computing has been speculated to be the next major revolution in computational technology. Thanks to intensive research and development by various academic institutions and big industry players, exciting progress has been made in achieving what has been claimed as "quantum supremacy."[209] At the same time, a closer examination of the quantum computing hardware reveals that the enormous size of these computers makes them analogous to the early days of digital computing (e.g. the Electronic Numerical Integrator and Computer, or ENIAC, in mid-1940s). A central issue that hinders the large-scale applicability of quantum computers is their scalability. Therefore, the use of advanced process technology used in microelectronics, which has driven the electronics revolution over the past several decades, has been proposed to promote integration and scalability in quantum computing hardware.

A. Highlights of III-N materials for application in quantum computing systems

From a materials point of view, the choice of a material platform with the desired properties of multi-functionality, easy integration, scalability, and reliable micro-fabrication is as important. Major material platforms developed in microelectronics include Si-Ge, III-V and III-N platforms, each at a different level of maturity in terms of microelectronics technology. While each of these platforms has its own unique strengths and limitations, the III-N material platform stands out as a unique material system with a combination of semiconducting, superconducting, and piezoelectric/ferroelectric materials in the same epitaxial stack. In terms of semiconductors, the III-N semiconductors are wide band gap materials and the presence of polarization-induced 2-DEG in heterostrucutres (e.g. AlGaN/GAN, AlN/GaN) with high mobility makes them attractive for high speed RF devices. Thanks to the wurtzite crystal structure, many III-N materials (e.g. III-N and its alloys) exhibit piezoelectricity or even ferroelectricity (e.g. ScAlN). AlN and alloys (e.g. ScAlN) have given rise to high performance MEMS resonators, which are being increasingly used in being coupled to phonon states and even for quantum memories[210–213] The acoustoelectric effect applied on 2-DEG has been used in demonstrations of nonreciprocal delay lines.[214] In terms of superconductors, materials like NbN and TaN have been used in demonstrations of superconducting devices like single nanowire superconducting photon detectors (SNSPDs).[215] The rapid development and deep understanding of these (standalone) devices lay a solid foundation for the use of III-N platform for quantum computing applications.

Furthermore, monolithic integration of these materials (of a variety of properties) and device technologies allows for not only observation of physical phenomena, but also from an engineering perspective, new opportunities in cryogenic hardware. The integration of III-N semiconducting/superconducting heterostructures has resulted in observation of Shubnikov-de Haas oscillations, and the exhibition of quantum Hall effect and superconductivity for topological quantum computing.[216,217] Superconducting qubits based on epitaxially grown and, recently, sputtered NbN/AlN/NbN Josephson Junctions have been demonstrated.[15,16,218,219] Epitaxial layer of NbN when grown on GaN exhibits a higher critical temperature (the temperature below which NbN behaves like a super conductor) of $\sim$16 K than that of grown on Si substrate.[220] This would provide higher margin for power dissipation and noise for the LNAs being used in a quantum computing system. Initial attempts at integration of electronics (transistors) and MEMS (acoustic wave resonators) have achieved promising performance.[221] Many of these results might still in the initial proof-of-concept phase, but nevertheless these spotlights point to the potential for integration in the III-N quantum computing platform.

B. Grand vision of "quantum computing-on-a-chip"

In order to enable quantum computing to revolutionize our lives and truly deliver an impact to our society, achieving so-called "quantum supremacy," or even equivalent performance to classical computers, is not sufficient alone. An important aspect in the roadmap for future quantum computing systems is the scaling up of existing prototypes beyond tens of (quantum) bits. Analogous to how solid-state components eventually replaced vacuum tubes in VLSI electronics, the breakthrough in quantum computing would eventually come from

FIG. 20: (a) Epitaxial structure used in the demonstration of an all-GaN complementary gate driver circuit. (b) Device architecture for all-GaN complementary technology. The enhancement-mode p-FET device is fabricated on the top two-dimensional hole gas at the GaN/AlGaN interface, while the enhancement-mode n-FET device is obtained by connecting to the two-dimensional electron gas at the bottom AlGaN/GaN interface. (c) Optical micrograph of an all-GaN complementary gate driver. (d) Voltage transfer curve of the driver. (e) Input and output voltages for a 35 pF load.[192,205,206] Reproduced with permission from IEEE Electron Device Lett. 41 (6), 820 (2020), IEEE International Electron Devices Meeting (IEDM), 4.6.1-4.6.4 (2019). Copyright 2020 IEEE, 2019 IEEE.

the development of qubits and associated components with potential for large-scale integration. This requires harnessing the strength of the microelectronics to speed up VLSI quantum computing. It would be even more impactful to have "quantum computing-on-chip," so that the quantum computers would be as ubiquitous as conventional electronics.

A primary bottleneck in realizing such a vision is the fact that quantum computers require deep cryogenic temperatures (< 1 K) to achieve operation with long coherence times. A simplified illustration of the various stages of the quantum computer is presented in Fig. 21(a). The electronics are often discrete, commercial off-the-shelf components and placed at stages with higher temperatures (≥ 4 K). While such a configuration is useful for proof-of-concept research and in the prototyping of quantum computers, there are clearly limitations in the further promotion of this technology.

In order to enable the qubit and associated electronics to be located "closer together", they would have to make certain compromises, notably in the temperature of operation. It is generally accepted that deep cryogenic temperatures in the mK range is highly desired for the qubit aspect, due to longer coherence time, higher fidelity etc. Until high temperature qubits become feasible from physics and engineering standpoints, electronics would need to "compromise" by going to lower temperatures of operation, which gives rise to the concept of "cryo-CMOS."[222] Significant efforts have been devoted to research in cryogenic CMOS electronics. In other words, development of qubits is only one aspect of the entire quantum computing project. An equally important area, and an area of significant interest to the microelectronics community, is the development of high performance RF electronics for the control and readout of qubits at cryogenic temperatures, in order to ensure accurate readout and achieve as high a level of integration as possible, the control and readout circuitry should be placed near the 4 K stage instead of at room temperature. Till date, Si CMOS, SiGe and III-V (mostly InP-based) technologies have been examined with promising performance.[223–226] TCAD simulation models involving effects at cryogenic temperatures (e.g. incomplete ionization) are also explored for such devices.[227]

The grander vision, perhaps by far the most ambitious and challenging, is the co-location of the qubit and electronics on the same chip. This requires massive engineering efforts in the qubit, electronic devices, interconnects, process integration, and chip packaging. There has been initial research towards this direction. For example, Si qubits (spin qubits) and circuits have been integrated on the chip using a commercial CMOS process.[228,229] Furthermore, qubits themselves need to be densely packed in arrays, possible with 3D integration, to achieve a dense chip. To that end, 3D integration of superconducting qubit arrays and superconducting through-silicon via (TSV) have been pursued.[230,231] Interconnects operational at deep cryogenic temperatures (<1 K) have also been reported.[232]

While the initial research is encouraging, several issues could be observed. This section focuses on the microelectronics aspect. Firstly, if qubits remain at deep cryogenic temperatures (mK), to what extent could we tolerate any degradation / variation in performance of the process technology at such temperatures? Secondly, this approach of integration only works for those qubits which are either based on silicon or another semiconductor, or which could be heterogeneously integrated to a semiconductor platform. This would narrow the pool the candidates for qubit technologies, for example to spin and superconducting qubits, where each qubit technology has its strengths and limitations. Thirdly, from a process integration perspective, special care needs to be taken to ensure subsequent processing (especially back-end-of-line) does not damage the qubits (e.g. thermal budget), which are generally less robust than the electronics. Last, but not least, from a practical perspective, how effectively would cloud-based quantum computing (based on current large-sized quantum computing systems at cryogenic temperatures) serve society's needs, vis-a-vis on-chip personal quantum computing systems? Nevertheless, these questions do not hinder the motivation and need for integrated quantum computing platforms, and that is where tremendous research opportunities lie for the quantum engineering and microelectronics communities.

C. Steps to achieving the vision of the III-N quantum computing platform

Figure 21(b) presents a summary of the highlights of the III-N platform for quantum computing applications. Having established the merits of the III-N quantum computing platform, this section briefly discusses some future areas of research in components and integration to realize such a vision.

a. Qubits It is obvious that high performance qubits, e.g. long coherence time, based on III-N would need to be realized. Previous work has demonstrated a superconducting qubit based on III-N Josephson Junctions.[15] There remains significant room for research on epitaxially grown (typically MBE) III-N Josephson Junctions, while Josephson Junctions based on device layer processing (as do many $Al/AlO_x/Al$ Josephson Junctions) would be much more desired for their flexibility in fabrication and ease of integration with other fabrication processes. For example, it is reported that high quality III-N superconductors could be deposited by DC reactive magnetron sputtering.[233] Other quantum computing technologies being actively explored for III-N include nitrogen vacancy (NV) centers.[234] Spintronics based on wide band gap III-N has also been explored, with the possibility of evolving into spin qubits in the future.[235–237]

b. Electronics Several highlights exist for GaN electronics in this area. From a materials perspective, the electron channel is induced by polarization, rather than by intentional degenerate doping.[238] This avoids potential issues in degradation of performance caused by degenerate doping.[239] From a scalability perspective, large-area (up to 300 mm) GaN-on-Si electronics has been demonstrated, where their RF and noise performance have been reported to be close to state-of-the-art Si and III-V technologies.[80]

Another flexibility of III-N electronics is the possibility of integration with other more mature electronics platforms, notably Si and SiC.[80,192,240] While monolithic integration of all quantum computing components on the III-N platform is highly desired to achieve compact size, easier fabrication and simplified packaging steps, the possibility of heterogeneous integration makes III-N electronics an "add on" module that could also be beneficial for other qubit platforms (other than superconducting qubits) like Si isotope spin qubits and SiC NV centers.[241] AlGaN/GaN HEMTs with NbN gates (Fig. 21(c)) have been demonstrated, opening the possibility of using the NbN layer for integration with other superconducting components, e.g. Josephson junctions.[242]

A significant challenge is the lack of the level of VLSI and compactness as compared to Si CMOS advanced nodes. This hinders the creation of more complicated circuits, especially required in the control and back-end readout (after signal amplification) stages. Nevertheless, GaN integrated circuit technology is rapidly catching up, as exemplfied by recent proof-of-concept demonstrations of analog, RF (other than traditional PAs) and power ICs.[243,244] With a growing demand for all-GaN microsystems, GaN ICs are expected to achieve a higher level of integration and with added functionalities. Furthermore, even if the cost of an all-GaN microsystem is prohibitively high, heterogeneous integration could be used, though not desired from a performance standpoint. In such cases, Si CMOS could be used for conventional electronics, but still integrated with GaN circuits on the same chip.

c. MEMS While MEMS components are not commonly found in today's quantum computing systems, III-N layers, especially AlN, GaN and alloys, are extensively used as functional materials in MEMS devices, spanning a wide range of applications including RF front-end filters, acoustic delay lines, timing reference, acoustic wave sensors, and even in the biomedical area.[214,245–248] There has been significant research on coupling between MEMS resonators modes and qubits, though it appears that it is at an early stage and there is a lot of room for development as various qubit technologies evolve over time. From a MEMS device perspective, it is insightful to study the operation of such device in deep cryogenic environments, in terms of material properties, resonator loss mechanisms etc.

The availability of piezoelectric properties in III-N materials is certainly a major highlight for the integrated III-N platform over other microelectronics platforms. The piezoelectric properties have been utilized in a wide variety of MEMS devices, including acoustic delay lines, RF front-end filters, acoustic wave sensors etc. Furthermore, the maturity of doped variants of piezoelectric nitride films (notably ScAlN which has ferroelectric properties) have led to renewed interest in the area of resonant MEMS for added functionality.[210,249,250] There has not been too much demonstrations in the cryogenic environments (operation environment of quantum computing systems), but it could be foreseen that the area of RF MEMS will receive increasing attention.

d. Justifying the need for an integrated platform Before the conclusion of this section, it is worthy to take a step back and revisit the fundamental question, the motivation for an integrated platform based on a single microelectronics material system. More specifically, the proposition that requires significant justification is the need for an integrated III-N platform (monolithic or heterogeneous integration), since many of the nitride layers in the devices and components (e.g. MEMS, SNSPD) are sputtered at the device layer, often on SOI platform.

It is evident that among all of the area of application of III-N, the absolute need for epitaxial growth (MOCVD/MBE) is the most critical for electronics (HEMTs). This is because these devices rely on 2-DEG at the AlGaN/GaN interface and based on current technology projections, only epitaxial growth (not sputtering) ensures single crystalline material and a high quality interface for a high mobility channel. There are also other highlights. For example, the superconducting properties of NbN, even if reactively sputtered, has been shown to significantly improve when deposited on GaN substrate. Epitaxial III-N MEMS resonators have been proposed and demonstrated to be highly coherent multi-phonon sources for quantum acoustodynamics.[211,251]

As with any technology, the merits of III-N materials for quantum computing and related applications need to be examined in the greater context of the necessity and feasibility of an integrated III-N platform (monolithic or heterogeneous integration). In the push for an integrated III-N quantum computing platform, research efforts in high performance and scalable III-N cryogenic electronics technology would be a major driving force that justifies the merits of the proposed III-N quantum computing platform. Once the electronics thrust of the proposed platform is established, the other devices which take advantage of III-N properties would fall in place.

VII. DEFECTS, FREQUENCY DISPERSION, AND RELIABILITY CONSIDERATIONS

Despite their impressive material attributes and potential for RF applications, the performance and reliability of GaN devices is limited by a number of degradation mechanisms whose physics must be carefully investigated and modeled to make this technology a viable platform for high-frequency electronics. For example, mechanical and thermal stresses induced via the inverse piezoelectric effect in the device at high electric fields close to the gate-drain edge can lead to physical gate degradation (cracking and surface pitting). In the on-state of the device, highly energetic hot electrons could generate new trapping centers, which would further lead to electrical and mechanical degradation of the device structure. Prominently, GaN devices suffer from dispersion effects due to which there exists a significant difference in their DC and RF performance metrics (i.e., the dynamic $I-V$ curves are different from static $I-V$ curves). The main cause of DC-to-RF dispersion in GaN HEMTs is related to carrier trapping via defects introduced either during the growth process or result from stress experienced by the device under high electric fields and junction temperature. The electrically active defects in GaN HEMTs capture and emit free carriers with a finite time constant that depends on their physical properties such as their activation energy, number density, and capture cross-section. During static $I-V$ measurements, the traps can easily follow the applied voltage signal at the terminals. However, if a voltage pulse with a time duration shorter than the time constant of trap charging/discharging is applied, the traps are unable to follow the input signal, thus resulting in a different set of dynamic $I-V$ curves. In the next sub-sections, we discuss the impact of defects in limiting the performance of GaN technology and recent research progress aimed at addressing critical issues related to device reliability. We also discuss the future need to develop a "computational tools" framework that integrates the physics of reliability with electro-thermal transport models, enabling the co-design of materials-devices-circuits and facilitating the insertion of GaN in the next-generation RF infrastructure.

A. Gate Leakage

Electrically active defects in GaN HEMTs can be intrinsic, such as gallium vacancy, or extrinsic, such as iron or carbon doping, point or extended (dislocation related), bulk, surface, or interface related, present under the gate or in access region, related to the buffer, barrier, or the passivation layer (see Fig. 22). Defects degrade the performance of GaN HEMTs in several ways. In the DC operation mode, defects enhance gate leakage due to Schottky interface issues or the poor insulator quality in metal-insulator-semiconductor (MIS) structures. Gate leakage lowers the breakdown voltage of the gate electrode and imposes significant burden on the design of the gate driver. As shown in Table I, gate leakage in GaN HEMTs can be tailored by employing a variety of surface passivation, surface treatment, and annealing techniques. Novel methods of reducing gate leakage, such as through the use of layered two-dimensional materials, are being actively investigated. In this regard, highly resistive fluorinated graphene has emerged as an excellent barrier material for the gate in metal-insulator-semiconductor (MIS)-HEMT structures. In Ref. 252, fluorinated graphene was inserted between Al_2O_3 gate dielectric and AlGaN barrier layer in GaN MIS-HEMTs to suppress gate leakage by two orders of magnitude. In another study, fluorinated graphene was employed as the barrier material between

FIG. 21: Highlights of III-N platform for quantum computing application. (a) Schematic of a superconducting quantum computing system, with a focus on the complex RF electronics at cryogenic temperature; (b) An overview roadmap illustrating how the wide variety of material properties (semiconducting, superconducting, piezoelectric) in the III-N family could be used in devices and subsequently building blocks in quantum computing systems; (c) An example of III-N integration, the NbN-gated AlGaN/GaN HEMT, showing the device structure, I-V characteristics and potential for low noise amplification.[242]

the gate electrode (Ti/Al/Au) and the AlGaN barrier in p-GaN HEMTs, which increased the on-off ratio by 500×, while also reducing the off-state leakage by 50×.[253] Early experiments on the use of layered boron nitride as the gate dielectric in GaN HEMTs have shown promising results.[254] Specifically, by inserting an amorphous α- boron nitride transition layer between hexagonal boron nitride and $Al_{0.25}Ga_{0.75}N$, dangling bonds and defects at the interface were minimized, thus resulting in high saturation current ($>$ 1200 mA/mm), high transconductance ($>$ 250 mS/mm), while the reverse (forward) gate leakage was suppressed by three (six) orders of magnitude compared to Schottky gate HEMTs. Very recently, Ga_2O_3 has been employed as a gate dielectric in Fin-channel arrays of GaN MOSHEMTs.[255] These devices exhibited low gate-source leakage (in the pA to nA range for $V_{GS} = -100$ V) and high gate-source breakdown voltage ($V_B = -540$ V) due to the superior insulating quality of Ga_2O_3.

From the perspective of circuit simulations, compact models that analytically establish the relationship between device output (gate leakage) and device inputs (gate bias, device geometry, operating temperature) are highly desired. In Ref. 263, a compact model was developed to investigate the physics of the gate leakage due to thermal emission (TE), trap-assisted tunneling (TAT), Poole Frenkel emission (PFE), and Fowler-Nordheim tunneling (FNT), and the model was applied to understand the correlation between process parameters and gate leakage physics for $Al_{0.22}Ga_{0.78}N$/GaN HEMTs up to 573 K.[263] In the reverse-biased mode, PFE and FNT emerge as the dominant leakage mechanisms due to the high electric fields across the top barrier. Figure 23 illustrates the various gate leakage mechanisms under forward- and reverse-

FIG. 22: Overview of the various traps and hot carrier effects that lead to dispersion and device degradation.

TABLE I: Impact of process flow on gate leakage in GaN HEMTs.

Process	**Impact on gate leakage (Value after gate optimization process)**	**Reference**
Oxygen passivation (200°C)	Reduced by $10^4\times$ (200 pA at $V_G = -5$ V)	256
O_2-plasma and HCl surface treatment and post gate annealing process (300°C)	Reduced by $10^7\times$ (2 pA/μm at $V_G = -30$ V)	257
Si_3N_4 passivation (300°C)	Reduced by $2\times$ (3.6 pA/μm at $V_G = -8$ V)	258
N_2O plasma treatment process for the recess gate	Reduced by $10^3\times$ (1 pA/μm at $V_G = -10$ V)	259
Non-alloyed regrown ohmic contacts	Reduced by $10^6\times$ (2 pA/mm at $V_G = -4$ V)	260
Post-metallization anneal (500°C) in Al_2O_3-AlGaN	Reduced by $10^3\times$ (20 pA/μm at $V_G = -5$ V)	261
Fluorinated graphene barrier between Al_2O_3 and AlGaN in GaN MIS-HEMT	Reduced by $10^2\times$ (1 pA/μm at $V_G = -8$ V)	252
Fluorinated graphene between gate (Ti/Al/Au) and AlGaN in p-GaN HEMTs	Reduced by $50\times$ (100 pA/μm at $V_G = -8$ V)	253
Layered α-/*h*- boron nitride gate dielectric	Reduced by $10^3\times$ (0.2 pA/μm at $V_G = -4$ V)	254
P-type gate doping via Mg diffusion + MgO formation to passivate surface traps	Reduced by $> 10^3\times$ (0.2 pA/μm at $V_G = 0$ V; < 650 pA/μm for $V_G < 0.4$ V)	262

biased modes of device operation. The TE and TAT mechanisms are active under both forward- and reverse-biased modes, while their relative contribution to the total gate leakage reduces under the reverse-biased mode. While the FNT is a one-step tunneling process, the TAT occurs in multiple steps due to the capture and subsequent emission of carriers via the defect states in the insulator. Results in Fig. 24 obtained using the model in Ref. 263 show a comparison of the measurement data and model-generated data of the gate leakage in both forward and reverse biased mode at different temperatures for the HEMTs fabricated at a commercial lab. At a fixed gate bias, the model correctly predicts the experimentally observed increase in gate leakage with temperature. For these devices, the PFE component of the gate leakage was insignificant compared to the TE, TAT, and FNT components over the entire range of temperature and bias values explored in these studies. Additional studies, both theoretical and experimental, for disentangling the contributions from various leakage mechanisms in GaN technologies over broad temperature and bias range, including in the off-equilibrium regime (i.e., high V_{DS}) are necessary to improve the reliability of GaN technology.

B. Buffer Leakage

Defects, such as buffer dislocations, caused by the growth of GaN on non-native substrates have been shown to result in buffer leakage via various microscopy techniques including scanning Kelvin force, scanning capacitance, and conductive atomic force microscopies. Moreover, GaN buffer is generally unintentionally doped with silicon dopants (n-type), which make it rather conductive and unsuitable for high-power and high-frequency applications. However, buffer leakage can be mitigated through compensation doping. For example, Fe or C dopants in GaN act as deep acceptor levels and render GaN semi-insulating by compensating the unavoidable background silicon donors. However, it has been shown that C-doped devices have significant dispersion with a dynamic on-resistance that is 3-4$\times$ higher than that in the DC case.[264] Hence, alternate methods to suppress buffer leakage, such as by separating the buffer from the 2DEG at the AlGaN-GaN interface are highly desirable. The carbon doping in GaN is also linked to the hysteretic instability in the output characteristics of the device, also known as the "kink effect", both at cryogenic and room temperature.

The kink effect in GaN devices appears under a slow drain bias sweep and is a small step change in the drain current at drain bias slightly above the knee region of the forward sweep, with little to no reduction on the reverse sweep. The kink effect in GaN devices has persisted despite the progress in surface passivation techniques indicating that surface traps are likely not the cause of the kink. Given that the kink appears at rather low drain bias voltages (i.e., 2 to 3 V above the knee), previous theories speculating impact ionization to be the likely cause are not plausible. Other mechanisms responsible for the kink effect in GaN under consideration include field-dependent de-trapping process into deep donor or deep acceptor states in the vicinity of the gate. However, conventional models of field-dependent de-trapping processes are unable to explain the required capture cross-sections in these theories. More recently, it was shown that the hysteresis associated with the kink effect was highly susceptible to changes in the concentration of carbon doping, which is affected by the changes in the growth condition. The magnitude of the kink is correlated to the carbon doping, its degree of self-compensation, and the band-to-band leakage paths, and is thus difficult to precisely tailor during the growth process. Epitaxial configuration in which the resistivity increases from the top to the bottom layer is optimum for low dispersion associated with trapping in the bulk of the epitaxy for C-doped GaN devices.[265]

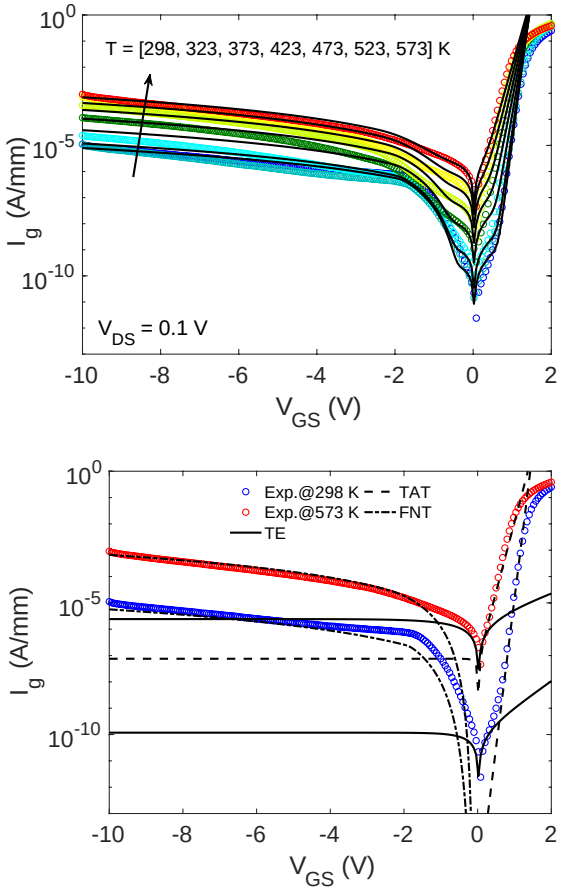

FIG. 24: (up) Gate leakage versus gate bias at different temperatures. Symbols indicate experimental data while solid lines correspond to model fits. The drain bias is fixed at 0.1 V. Reproduced with permission from the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2020. Copyright 2020 IEEE. (bottom) Contribution to gate leakage at 573 K and 298 K arising from trap assisted tunneling (TAT), Fowler Nordheim tunneling (FNT), and thermionic emission (TE).

FIG. 23: Components of gate leakage in AlGaN/GaN HEMTs under (a) reverse biased mode with $V_G < 0$ and (b) forward biased mode ($V_G > 0$). Here, V_G is the gate bias, $E_{\rm fm}$ and $E_{\rm fs}$ are the Fermi levels in the metal and semiconductor, respectively, and E_c is the bottom of the conduction band. TE: Thermionic emission, FNT: Fowler-Nordheim tunneling, PFE: Poole-Frenkel emission, TAT: Trap-assisted tunneling. Reproduced with permission from the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2020. Copyright 2020 IEEE.

C. Trap Dynamics and Impact on RF Operation

During RF operation of the device, traps cause effects such as gate lag, drain lag, knee walkout, and current collapse. Gate lag refers to the slow variation or long time delays in the drain current transient following gate voltage switching. In the case of drain lag, a change in drain voltage results in slow transient response of the drain current occurring over seconds. Additionally, a comparison of the pulsed and DC $I-V$ curves of GaN HEMTs reveals that the transition of the device operation from the linear to the saturation regime occurs at higher drain-source bias. This phenomenon is referred to as knee walkout. Finally, current collapse occurs when the drain current under pulsed conditions from pinch-off to on-state fails to reach the DC drain current values due to the traps possibly located at the edges of the gate.

At large reverse gate bias, the tunneling of electrons from the gate into the AlGaN barrier and their subsequent capture by the surface/interface states in AlGaN forms the so-called "virtual gate" in the drain-side access region, which reduces the 2DEG charge and the drain current in gate lag measurements. The lateral tunneling of electrons from the gate to the drain access region is facilitated by threading edge dislocations surrounded by space charge. Electrons tunnel into unoccupied states in the space charge under finite electric field and can move between dislocation sites either via hopping or thermal activation (the so-called percolation model), resulting in surface conduction as observed experimentally. The trapping of electrons in the buffer region leads to threshold voltage shift ($\Delta V_{\rm th}$), as well as dynamic $R_{\rm ON}$ and g_m change in the gate-drain access region. Gate lag increases as the reverse bias on the gate is increased as the virtual gate extends deeper into the access region. After the removal of the negative gate bias, the recovery of the drain current occurs on a timescale that is characteristic of the emission time constant of the traps. In measurements, the drain current transient in

on-state (e.g., $V_G = 0$) is monitored at various temperatures to extract the trap characteristics including its time-constant, activation energy, and capture cross-section.

To quantify the impact of the drain bias on gate lag and the recovery of the drain current at $V_G = 0$, measurements are performed by varying the drain-source bias in a HEMT structure. With an increase in the drain-source bias, the electric field in the gate-drain access region is enhanced, which lowers the activation energy of the trap states by several 100's of milli-eV due to the electric field crowding in the gate-drain access region.

Gate lag can be alleviated to a certain degree by using field plates to tailor the electric field profile in the gate-drain access region and via passivation of the AlGaN surface using dielectric layers such as SiN_x, SiO_2, Sc_2O_3, and HfSiO. Prior studies have suggested that surface passivation mitigates the dispersion effects, suppresses surface and barrier leakage,[266] while also increasing the 2DEG charge in the GaN channel. The latter is attributed to the build up of a fixed charge in the passivation layer, which stabilizes the surface upon charge trapping and increases the 2DEG in the channel.[267] However, other works have shown that surface passivation techniques only modulate the interaction of gate contact and surface traps without reducing the trap density.[268] Reference 269 employs source field plates to reduce trapping due to surface traps and improve the reliability of GaN HEMTs for high-voltage operation. More recently, the collective role of surface and buffer traps on modulating the channel electric field in GaN HEMTs and its breakdown voltage were probed using experimentally calibrated computational models.[270] It was found that the breakdown strength of GaN HEMTs was strongly affected by the presence of surface traps, while a shift in the breakdown hot-spot from the drain edge toward the gate edge was also found with an increase in surface trap density.

Transient spectroscopic methods to study traps in AlGaN/GaN capacitors and HEMTs include capacitance deep level transient spectroscopy (C-DLTS), capacitance deep level optical spectroscopy (C-DLOS), and drain current transient (DCT) spectroscopy. Due to measurement limitations, C-DLTS is capable of probing trap states that are within 1 eV of the band edge. C-DLOS is typically employed to probe traps located deeper in the bandgap. Here, the transient photocapacitance gives information related to the optical cross-section of the trap. The main limitations of C-DLOS and C-DLTS are that they are performed in diode or FAT-FET structures and, therefore, do not provide details of virtual gating in HEMT structures. The double-pulse DCT spectroscopy can be performed in three-terminal HEMTs and thus provides a more realistic assessment of the physical location of the dominant traps. For example, if the dominant trap in the device is located under the gated region, the pulsed $I-V$ characteristics will display a lower saturation current than their corresponding DC values since the traps located under the gate cause a time-dependent shift in the threshold voltage of the transistor. On the other hand, if the pulsed $I-V$ measurements reveal an increase in on-resistance of the device, then traps located in the gate-drain access region are likely involved.

In summary, to diminish the effect of traps, optimized growth and surface passivation techniques that reduce the dislocation density in the device are required. New metrology and spectroscopic techniques are also needed to quantify the impact of growth techniques on the origin and physical characteristics of defects and further combine this information with physics-based modeling to understand how traps impact device behavior in practical operating scenarios.

D. Reliability and Physics of Operation in Extreme Environment

Reliability and time-dependent degradation of the underlying transistor technology has emerged as a major concern, as it reduces the operational lifetime of high-frequency communication and sensing infrastructure. Unfortunately, the identification of the fundamental causes of device failure typically requires time-consuming and expensive testing and validation after test structures have been fabricated. Besides, the time and expenses incurred, results from reliability measurements are often fitted to empirical models which are unphysical and do not provide a link between materials science, physics, and time-dependent circuit failure.

As discussed in the previous sub-section, in the case of GaN HEMTs, a wide variety of degradation mechanisms have been noted such as surface pitting, reverse piezoelectric effect, charge trapping, hot electron phenomena, ohmic contact degradation, and sudden reduction of functionality. All reliability reports to date show evidence of more than one degradation mechanism in any given foundry's GaN technology. Hence, measuring an average degradation rate is difficult as the contributions to degradation from different mechanisms vary with time. This situation is exacerbated for operation in extreme radiation environments as they are quite difficult to replicate satisfactorily in an experimental laboratory. Toward this, a Monte Carlo simulation of how radiation interacts with matter could provide key insight into degradation processes pertinent to harsh environments. Examples of Monte Carlo simulators used for radiation transport and energy deposition include COSMIC,[271] MCNPX,[272] CUPID,[273,274] SEMM/SEMM-2,[275,276] and FASTRAD.[277] Monte Carlo-based assessment of radiation effects go beyond analytical computations that are mainly suited for legacy technologies. However, the speed and cost of implementation of Monte Carlo methods becomes prohibitive in several scenarios.

During the nominal operation of GaN HEMTs, the electric fields and carrier temperatures can vary by orders of magnitude, which can rapidly increase the temperature of electrons and lead to the generation of hot phonons with temperature around 2000 K. In fact, due to the very high electric fields in the gate-drain region under the saturation mode, most of the highly energetic electrons are promoted to the upper valleys like $L-M$ or Γ_2 and create the so-called hot spots of the device. The presence of hot carriers and rapidly varying electric fields in HEMTs creates additional point defects in the crystal, especially if there were pre-existing point defects formed during the growth of the heterostructure, and thus promotes new failure mechanisms and reduces the component's mean

time to failure.

To understand and tailor hot carrier phenomena and improve reliability of GaN HEMTs in the presence of large gradients of electric fields and temperature, and strong radiation, new computational models are highly desired. First, the physics of matter when driven far-from equilibrium cannot be captured using statistical methods and first-order transport equations typically fail to capture key carrier dynamics. In equilibrium, the distribution functions of electrons and phonons are described by the Fermi-Dirac and Bose-Einstein statistics, respectively. However, under non-equilibrium conditions which are to be expected in extreme environments, such as cyclic wide-temperature range environments, the distribution functions assume a significantly different shape. This means new and advanced computational methods to accurately handle the time-domain response of non-equilibrium matter must be used.

There is an emergent need to develop new models and methods to evaluate the impact of key stressors, such as large gradients of electric field and temperature and strong radiation, on device degradation during its operation under extreme environment. Temperature also influences the dynamics of trap occupancy and is thus expected to accelerate the degradation of transistor parameters, while also promoting new failure mechanisms. The link between stressors and device technology (i.e., materials and geometry) will provide fundamental insight into the time evolution and aging of ultra-high-frequency devices and their communication systems. For example, the stressors will determine the change in fundamental material characteristics (i.e., mobility, thermal conductivity etc.), which in turn will impact the $I-V$ characteristics. Such a model should also be able to predict the time evolution of stressors and consequently its impact on the time evolution of device output (i.e., the $I-V$ characteristics). Existing modeling techniques based on the drift-diffusion transport theory must be amended to cater to the ultra-scaled dimensions of next-generation GaN devices designed to achieve cut-off frequencies exceeding several 100's of GHz (see related discussion in Sec. VIII). This will necessitate using full band Monte Carlo simulations and the hydrodynamic formalism to treat the subsystems corresponding to free carriers, traps, and the lattice separately as the device is driven out of equilibrium. This approach will provide an in-depth analysis of the temperature profile of the device subject to the knowledge of its thermal resistance. Existing models in this regard treat thermal resistance empirically, thus lacking the connection between device performance, degradation, and key material and layout parameters. Apart from the creation of hotspots and thermal runaway challenges, large temperature excursions also fundamentally change the dynamics of traps. Therefore, new insight into the interaction between thermal and electric field gradients and trap characteristics will be needed toward enabling a reliability aware computational framework. With this perspective, the goal of future research must include:

- Development of a new computational framework to jointly model transport and heat conduction, trap dynamics, and interaction of radiation with matter that critically impact lifetime and device aging. By identifying and controlling key stressors (large excursions of temperature and field gradients and radiation dose), future research will enable the widespread deployment of GaN for new commercial application.
- Strengthening our understanding of degradation mechanisms and interpretation of experimental data. As such, theoretical research should form the basis of fabrication of non-canonical device structures that are inherently more robust and can meet the power- frequency requirements of 5G and 6G systems over a broad range of operating conditions including those that are harsh and extreme.
- Enabling a circuit designer to make informed decisions on performance-reliability tradeoff based on their specific application.

VIII. SIMULATION FRAMEWORK FROM DEVICE-LEVEL TO CIRCUIT-LEVEL FOR NOVEL GAN DEVICES FOR RF AND CMOS APPLICATIONS

In real-world applications, most electronic devices will need to be eventually integrated into systems to perform useful functions. For example, an AlGaN/GaN HEMT is integrated into a MMIC PA to perform power amplification. While device-level research is critical to improving the device performance, an appreciation of the circuit-level application is equally important. A simulation/modeling framework needs to be established to ensure that the device-circuit interaction is well studied, in particular for novel devices under research. This section briefly presents the developed simulation framework, covers two examples of novel devices whose circuit-level performance is estimated, and offers perspectives on areas of future research into this framework.

A. Motivation for such a simulation framework

1. *Achieving a higher level of abstraction at each level*

VLSI is centered on the concept of achieving a higher degree of abstraction at each higher level of the architecture. In this bottom-up approach, a central theme of the device research community is to deliver higher performance devices with applications at the microsystem level, in order to fundamentally improve the performance of the microsystem. To that end, innovations in device designs and optimizations to existing structures would need to be studied, paying close attention to the application context (e.g. RF, power, logic circuits). For this bottom-up approach to deliver a genuine impact at the microsystem level, an experimentally calibrated, accurate, easy-to-use simulation methodology from device-level to circuit-level is necessary.

Traditionally, device R&D, in particular for silicon devices, has been aided by the extensive use of TCAD software (e.g. Silvaco™, Synopsys Sentaurus™) to study the device mechanism, understand device characteristics, and to propose new

device ideas. These softwares make use of theoretical (e.g. classical quasi-electrostatics based on Maxwell's Equations) and empirical/fitting models (e.g. mobility models) to perform finite-element method (FEM) calculations on device structures. First principle calculation based on condensed matter physics is typically not required for many of the standard device structures, therefore achieving a higher level of abstraction. One challenge in the TCAD of newer (non-Si) materials is the need for accurate physics models to capture the device mechanism. This is partly hindered by the variability in material growth conditions (e.g. buffer traps and variation in 2DEG mobility behavior) and the need for further understanding of reliability issues in these newer devices (e.g. hot carrier effects, impact of surface states). With the constant improvement in material quality and uniformity, the models could be more accurately constructed at the device-level.

The widespread adoption of GaN electronics offers strong motivation for the VLSI of GaN electronics at the circuit-level and possibly even microsystem-level. This is made possible largely thanks to industrial efforts in the scalability of GaN technology, therefore allowing proof-of-concept demonstrations from academic research to be rapidly scaled up to create impact at the circuit-level. Furthermore, at the circuit-level, drawing lessons from the highly successful VLSI of Si CMOS technology, reliable and accurate compact models are required so that the circuit simulator could quickly solve complicated circuits, instead of resorting to solving Maxwell's Equations for every transistor or diode!

2. *Device-Circuit Interaction*

Increasing attention has been paid to device-circuit interaction, a "give-and-take" approach between device and circuit designers, as opposed to the traditional approach of circuit designers "taking" (maybe even forced to accept) whatever existing devices could offer. This field is especially exciting for materials like GaN where at the current stage of maturation of technology, there is significant research activity at *both* device and circuit levels.

A method of studying device-circuit interaction is mixed-mode simulation offered in many device-level TCAD softwares, which is self-consistent simulation of a device whose electrodes are connected to a circuit. Mixed-mode simulation is evidently a natural extension of traditional TCAD (device-level) simulation and has been adopted by many device-level researchers for novel devices.[99,278,279] In such a simulation methodology, the optimization of device-level parameters is more direct, in particular for novel devices which have significant flexibility in design space, e.g., vertical devices. Furthermore, even minor details in device characteristics will be captured directly at the circuit-level. This is typically the case for simpler circuits where device-level performance directly impacts the circuit-level characteristics, for example, digital logic building blocks, simple power converter topologies etc.

While mixed-mode simulation offers some convenience to the device designers, some limitations are evident. Significant amounts of computational resources are required for such a self-consistent simulation. Convergence would be tricky to achieve. More importantly, under the context of increasing R&D in GaN ICs, the device-centered mixed-mode simulation technique lacks scalability for VLSI. A variety of GaN ICs have been demonstrated in 200 mm wafers.[243,280,281] In order to further propel the design of GaN ICs and also devices for such ICs, a scalable simulation methodology is evidently required.

B. Three-step methodology from device-level to circuit-level simulation

The three-step methodology is illustrated in Fig. 28(a). Firstly, device-level simulation is performed using TCAD softwares. Important characteristics to be extracted are *I-V* and *C-V*. For experimental devices, the measurement data could also be used. Next, a compact model is created which accurately captures the device-level simulation. This compact model is then placed into a circuit simulator (e.g. Cadence Virtuoso, Keysight ADS) to perform circuit-level simulation.

1. *Compact Device Modeling*

In the three-step methodology, compact modeling serves as the bridge between the device-level and circuit-level. From a design design research perspective, compact models aid the physics-based understanding of the device, are straightforward to use, and have been successfully applied to analyze several RF and power IC applications.[172,282–284]

Compact models are developed with a goal of faithfully reproducing the device terminal behavior (charges and currents) over a broad range of operating conditions, i.e., terminal voltages and temperatures. Physically derived compact models provide an intuitive insight into device- and circuit-level limits and opportunities and are thus preferred for circuit simulation and by device technologists as a substitute for computationally complex and intensive TCAD simulations. Moreover, physics-based compact models offer predictive capability to quantify performance of the device and its impact on circuit behavior with technology evolution (Fig. 25). The model parameters contained in a compact model must be extracted by fitting the model to the measured large-signal and small-signal response of the device. Along with experimental data, TCAD-generated data could also be used for model validation since it enables the testing of specific model features for which experimental data is not readily available. Additionally, TCAD simulations can allow us to probe spatially resolved carrier transport and electrostatics in the device structure, thus providing higher-resolution datasets for compact model validation, as well as for strengthening the model physics.

For analog GaN transistors, the Compact Model Council (CMC), part of the silicon integration initiative (Si2), shortlisted eight compact models during their GaN-model evaluation and standardization efforts. CMC activities in this regard can be found in Ref. 285. The CMC has recently standardized two GaN compact models to be used within industrial ana-

log and RF simulation tools: (1) the MIT Virtual Source GaN model for RF (MVSG-RF) developed at the Massachusetts Institute of Technology in 2016[286] and (2) the Advanced Spice Model for High-Electron Mobility Transistor (ASM-HEMT) developed at U.C. Berkeley in 2016[287].

Salient features of prominent III-V and GaN HEMT compact models are compared in Table II. Prior to the standardization effort by CMC, typically models for GaAs and InP, including Curtice, EEHEMT, HSP, and Angelov models, were adapted to GaN HEMTs. Major weaknesses of earlier models include their inability to capture device physics accurately and a complex extraction flow due to the presence of several non-physical parameters. As the number of empirical and non-physical parameters in a device model grows, the cost of parameter extraction becomes prohibitive. In this case, it becomes necessary to modify the extraction flow for different process technologies and geometrical variations in the device.

The ASM-HEMT GaN model adopts a surface-potential-based approach to derive the drain-source current assuming the validity of the gradual channel approximation (GCA) throughout the channel. Owing to its threshold-voltage-based approach to obtain the inversion charge and the channel current, MVSG-RF offers a higher degree of mathematical robustness and less complexity compared to the ASM-HEMT model. Carrier trapping, which results in distinct DC and RF device characteristics, is included as a sub-circuit, integrated with the core implementation, in both ASM-HEMT and MVSG-RF models. The ASM-HEMT uses previous works[288,289] on the Shockley-Read-Hall recombination of a defect state to compute the potential associated with the trap center, which in turn is used to modify three core model parameters, namely the cut-off voltage, the mobility degradation coefficient, and the 2DEG areal charge density in the drain access region. On the other hand, in MVSG-RF, an average charge-trapping module comprising a low-pass RC filter is used to increase the sheet resistance of the drain access implicit transistor, thus mimicking the knee walkout observed in GaN devices. The source function of the RC circuit is empirically modeled in terms of the voltage stressors of the device, i.e., the drain-gate bias, and the channel temperature. Here, the trapping and de-trapping time constants are assumed to be identical, which although not physically correct, offers the benefit of a simpler sub-circuit implementation. To model the trapping-induced dynamic change in the threshold voltage of the GaN HEMT, the MVSG-RF uses diode-capacitance subcircuits with an empirical source function based on the drain-gate bias. The presence of diodes differentiates between trapping and de-trapping processes and is thus a more accurate representation of the device physics.

While both ASM-HEMT and MVSG-RF models have been successfully applied to industrial GaN devices, they have a few shortcomings. For example, these models ignore the effect of voltage-dependent density-of-states and other quantum mechanical effects that exist in thin channel devices. Moreover, both MSVG-RF and ASM-HEMT models are strictly applicable to long-channel devices in which the transport can be described within the drift-diffusion (DD) theory. Indeed, the last decade has witnessed impressive progress in terms of channel length scaling ($L_{\text{eff}} < 50$ nm) and nanostructure-based designs of GaN HEMTs to improve the RF performance. Measurements have shown that the low-field diffusive mobility of electrons in these structures is $\sim (1250-1650)$ cm^2/Vs at room temperature. This implies that the non-degenerate mean free path (MFP) of electrons is around 50-70 nm in these devices,[290] which is comparable to their effective (gated) channel length. In such scaled devices, quasi-ballistic (QB) transport becomes important and the GCA is only valid at the top-of-the-barrier (ToB). Essentially, GCA assumes that the vertical electric field is much greater than the lateral electric field throughout the channel length. Calculations such as those conducted in Ref. 291 show that the validity of GCA throughout the channel is questionable in QB transport even for small V_{ds}. Previous computational studies have also shown that in QB transport, when channel length and carrier MFP are of the same magnitude, the distribution function is no longer Maxwellian and "ballistic peaks" appear in the velocity distribution.[292] Therefore, DD models, which assume that the distribution function is a shifted Maxwellian, cannot accurately describe the physics of scaled transistors. Moreover, in GaN devices operating at cryogenic temperature (4.2 K), the diffusive electron mobility can exceed 10,000 cm^2/Vs,[293] which means that the mean free path of electrons is in the micrometer regime. In this regime, the ASM-HEMT, MVSG-RF, and other modeling approaches would fail even for GaN HEMTs with gate lengths of several 100's of nanometers since QB transport is found in devices with $L_{\text{eff}} \lessapprox \lambda$. Based on the above discussion, it is evident that new analytic models that capture the essential physics of quasi-ballistic transport in GaN HEMTs are key toward facilitating the technology-device-circuit co-design.

A new compact model based on the Landauer's transport theory[294] published by the co-author Rakheja preserves the essential physics of transport in ultra-scaled GaN devices with QB transport. The model adopts a transmission viewpoint of current, which has profoundly impacted the understanding of basic physics of transport. Conventional semiconductor transport was initially formulated using this theory by McKelvey and Shockley.[295] An exhaustive validation of the self-consistent dynamic-static Rakheja-Li model was conducted for devices with aggressively scaled gate lengths of 20 nm, 42 nm, 50 nm, 105 nm, and 150 nm. The detailed descriptions of these devices can be found in Refs. 296 and 297. Figure 26(a,b) shows the model validation against AlN/GaN/AlGaN HEMT of gate length 20 nm and gate-source and gate-drain separation of 70 nm. These depletion-mode devices were were fabricated via molecular beam epitaxy on a 3-inch SiC substrate. The model shows excellent agreement with the measurement output and transfer curves of the devices over broad bias. The model was also matched against TCAD $I-V$ simulations conducted for nearly self-aligned GaN HEMTs with gate length of 50 nm, and the model agrees well with the numerically simulated results as shown in Fig. 26(c,d).

In addition to static transport validation, the Rakheja-Li model was applied to study the C-V measurements of deeply scaled GaN HEMTs [$In_{0.17}Al_{0.83}N$ (7.4 nm) | AlN (1nm) |

FIG. 25: Overview of modeling and simulation approaches. Compact device models enable large-scale circuit simulations with several interconnected transistors, thus enabling a way forward for technology-device-circuit co-design and co-optimization.

Model	Approx. no. of parameters	Geometry scalability	Electro-thermal	Trapping	Mathematical robustness^{+}	Original device context
Angelov	90	Yes (empirical)	No	Yes (empirical)	Good	HEMT/MESFET
Curtice$^{\#}$	55	Yes (empirical)	Yes	No	Partial	LD MOSFET
EEHEMT	71	No	Yes	No	Poor (piece-wise)	HEMT
HSP-LETI$^{\#\#}$	35	Yes (empirical)	Partial	No	Partial	GaN HEMT
ASM-HEMT	212	Yes (empirical)	Partial	Yes (empirical)	Good	GaN HEMT
MVSG-RF	109	Yes (empirical)	Partial	Yes (empirical)	Good	GaN HEMT

TABLE II: A comparison of the salient features of various compact models targeted for III-V and GaN HEMTs. Earlier models (unshaded cells) were primarily developed for III-V and InP devices, while the recent models (shaded cells) were developed for GaN technology. $^{\#}$Other variants of Curtice model include CHEMT and CFET, but were developed for GaAs FETs. $^{\#\#}$Model does not include non-linearity in access regions and applicability to RF simulations is not clear. $^{+}$Mathematical robustness is defined with respect to DC Gummel symmetry and AC McAndrew symmetry tests, as well as convergence in frequency- and time-domain circuit simulations in both forward and reverse-biased modes.

GaN (26 nm) | $In_{0.15}Ga_{0.85}N$ (3.3 nm) | GaN | SiC (buffer)] fabricated at MIT. The model validation of gate capacitance (C_{gg}) for 42-nm and 105-nm gate-length devices is shown in Fig. 27. Due to its ability to accurately account for the fringing capacitances as the device transitions from off-state to on-state, the model correctly reproduces C_{gg} and C_{gd} data of fabricated devices over a broad gate and drain bias range.

While the existing compact models (ASM-HEMT and MVSG-RF for DD transport and Rakheja-Li for QB transport) can aid in evaluating the device-circuit interactions, further research is needed to expand the scope of these models. Compact models generally have a tradeoff between computational complexity and accuracy of physics. Hence, the ASM-HEMT and MVSG-RF models only incorporate a limited number of thermal and trapping nodes to represent time constants of these processes. However, in a practical device, both thermal and trap-related charging/discharging processes involve sum of several exponentials and thus require more than one circuit node to be properly accounted for. Future efforts in this direction must explore techniques to minimize the computational burden, while also capturing the essential device physics. Existing modeling frameworks must be amended to handle operation at ultrahigh frequencies where non-quasi-static (NQS) effects in the device must be included. That is, when the transistor is driven by signals with a very fast rise time, shorter than the transit time of carriers through the channel, then the assumption that the channel charge is a function only of terminal voltages does not hold. The NQS operation is typically represented by adopting a distributed channel model, where the transistor is partitioned into n smaller channel length tran-

FIG. 26: Model fit to the output characteristics (a) and transfer characteristics (b) reported in Ref. 298. Model fit to the output characteristics (c) and transfer characteristics (d) for self-aligned device simulated using Sentaurus. The structure consists of 24-nm thick $Al_{0.3}Ga_{0.7}N$ on GaN. Both source-gate and drain-gate access regions are scaled down to 50 nm, which is similar to the structure in Ref. 298. Solid lines are model fits, while symbols correspond to experimental data.

FIG. 27: Validation of the Rakheja-Li model against the C-V measurements of devices fabricated at MIT.[297] Symbols correspond to measured data, while solid lines correspond to model fits. Reproduced from Journal of Applied Physics, 125(13), 134503, with the permission of AIP Publishing.

sistors. However, such a representation naturally imposes significant computational burden and has thus been challenging to implement for GaN transistors. Other new research areas in compact modeling of GaN transistors include incorporating memory effects such as the V_{th} drift and initial condition dependence of V_{TH}, as well as modeling basic model parameters such as DIBL, V_{TH}, and non-ideality in terms of technology and geometry parameters. Further development of such physics-based models will enable the co-designing and co-optimizing across the design hierarchy and ultimately establish the connection between circuit- and architecture-level research and research aimed at optimizing individual devices for RF applications, as well as digital, CMOS, and cryogenic applications of the future.

An alternative method of compact modeling is the fitting of small-signal parameters (e.g. g_m, C_g) and using this custom-built small-signal model for large-signal simulation, similar to the Angelov model, an early model for HEMTs.[299,300] This method has been recently used in large-signal simulations for power and linearity[301,302]. While this is useful in capturing non-conventional small-signal behavior (like in the graded channel FET), it can be more time consuming and it remains to be seen how this method could be rapidly adopted by the wider device community.

C. Use of three-step methodology for novel GaN devices

Some examples of the use of three-step methodology for novel GaN devices are illustrated in Fig. 28(b)–(e), including p-GaN gated AlGaN/GaN HEMT (using self-aligned process and high temperature robust technology), GaN vertical FinFET intended for RF application, and GaN CMOS.

1. GaN vertical fin RF transistors

Thanks to the high current handling capability, more uniform heat generation, and high breakdown voltage for given chip area, the vertical device structure has been proposed for high power and high frequency applications. GaN vertical FinFETs have been demonstrated for power switching application, and they are actively explored for high power RF amplification. The vertical FinFET was modified to make them suitable for RF operation (e.g. quasi-vertical structure), but with any new structure, it is important to estimate the potential of such a structure for the circuit-level application. With the aid of the three-step methodology, simulation of the proof-of-concept device in a GaN PA shows promising performance at the K_a band.[161] Experimental work of these devices is ongoing.

FIG. 28: (a) Device-level to circuit-level simulation framework which is performed using a three-step methodology.[206] Good fit to two types of novel GaN devices, namely (b) p-GaN gated AlGaN/GaN HEMT featuring a self-aligned process and high temperature robust technology; (c) GaN vertical FinFET optimized for RF application. (d) Using the methodology described in (a), a GaN complementary logic inverter was accurately modeled. For the first time, GaN p-FETs were modeled. (e) The logic inverter model illustrated in (d) was used to estimate the performance of such a GaN CMOS technology, both at room temperature and at high temperature (300°C). A 43-stage ring oscillator was chosen due to its significance in digital VLSI technology. The delay per stage can be improved by increasing the current density of GaN p-FET which is an active area of research. Possible areas of applications for such technology include (i) the high temperature logic intended for space and geothermal applications, (ii) on-chip power converters, and (iii) active interposer. where the circuits operate in the range of hundreds of kHz to MHz. The results in (b)–(e) indicate that the device-level to circuit-level simulation framework proposed in (a) is capable of modeling, estimating circuit-level performance and studying device-circuit interaction of novel GaN-based devices. Reproduced with permission from 2021 Device Research Conference (DRC), 2021. Copyright 2021 IEEE.

2. GaN CMOS

GaN p-type transistors, in particular those developed on scalable GaN CMOS platforms, have received significant attention in recent years, not only because of its novelty and improving performance, but more importantly, because of the tremendous potential for future GaN CMOS circuits.[192] Even though discrete p-type and n-type transistors were developed early, the integration technology of both of these components remained challenging, particularly in the context of university fabrication facilities.[206] In this work, the logic inverter behavior was predicted based on the three-step methodology involving the MVSG modeling of p-FET and n-FET on the regrowth-free GaN complementary logic platform. In the later experimental demonstration of such a logic inverter, the measured DC transfer result was found to closely resemble the simulated characteristics (refer to Fig. 28(d)).[192]**?** This proves that the key characteristics of the newly developed devices (p-FET and n-FET on the GaN CMOS platform), e.g. threshold voltage, relative current levels, have been taken into adequate account in the compact models and subsequently the circuit-level simulation. The GaN CMOS simulation framework was scaled up to estimate the performance of digital logic building blocks (including ring oscillator, shown in Fig. 28(e), and 6-T SRAM) in room temperature operation and at high temperature (300° C) operation.**?** This work highlights the use of the three-step methodology to develop a scalable simulation framework which would be beneficial for future developments of GaN CMOS technology.

D. Accurate device-level models and scaling Up Simulation Frameworks for GaN PDKs

With the widespread adoption of GaN electronic devices, increasingly accurate models which could incorporate the details of the device operation, e.g. transient switching behavior for power switches, are highly desired. In recent years, modeling techniques such as Keysight DynaFET, and use of neural network and Bayesian inference for accurate modeling have been developed.[303–305] In the case of GaN power switches, they are being operated at higher frequencies (>10 MHz) so traditional microwave concepts like S parameters are used to model these high frequency switches. At the same time, other academic research efforts are focused on developing unified compact models for GaN transistors which aid our physical understanding of the device operation.[296,297,306,307] There is significant work at the device-level to constantly improve our

understanding of the device operation.

In order to realize the vision of VLSI for GaN electronics, there is an significant need for the development of process design kits (PDKs), in particular for the new technologies like GaN CMOS which have significant potential for being scaled up, and which would only realize their true potential through being scaled up (as opposed to discrete GaN p-FETs). The PDKs would make GaN device technology more accessible to circuit designers. The use of three-step methodology could play a role in the development of PDKs by linking the device-level characteristics to circuit-level performance.

IX. CONCLUSIONS

We provided a review and glimpse of the future of GaN-based device and circuit technologies for applications in power electronics, RF electronics, and digital and quantum electronics and the potential for their cross-fertilization. For power electronics, we provided a perspective on high-to-low voltage, vertical and lateral, 2D and 3D, and multi-channel device structures, as well as discussed the dynamic and robustness issues of GaN devices. The potential of GaN for digital PAs and the integration of software, hardware, and AI approaches can lead to highly optimized circuits and systems for future mm-wave operation. We presented our vision on going beyond the traditional power and RF applications of GaN and enabling a new era of GaN-based digital and quantum electronics. The need for an integrated approach for the co-design and co-optimization across the design stack, from materials to devices to circuits and systems, is strongly emphasized. We held the viewpoint that model-based design and simulation is a crucial element to reduce the cost and turn-around time of protyping and ultimately deliver a heterogeneous platform with densely integrated components for new and exciting commercial applications of GaN technology.

AUTHORS' CONTRIBUTION

K. H. Teo, Y. Zhang, N. Chowdhury, S. Rakheja, and R. Ma contributed equally to this work.

DATA AVAILABILITY STATEMENT

The data that supports the findings of this study are available within the article.

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