MITSUBISHI ELECTRIC RESEARCH LABORATORIES
https://www.merl.com

Full-Range Three-Stage 16GSa/s Riemann Pump RF-Power DAC in GaN HEMT

Furuichi, Tomoyuki; Ma, Rui; Koike-Akino, Toshiaki; Komatsuszaki, Yuji

TR2021-141 December 22, 2021

Abstract

In this study, we proposed a new encoding method to reduce power consumption and expanding the bit resolution of Riemann Pump (RP) digital-to-analog converters (DAC). In addition, a new circuit topology was demonstrated enabling highside and low-side GaN transistors to operate independently such that the power consumption is significantly reduced by preventing unnecessary current flow. Moreover, our design realizes higher bit-level compared with the state-of-the-art complementary encoding method. We designed and fabricated a 3.9-bit RP using 0.15um GaN process to validate its performance benefit. The simulation with practical device models confirms that our design can reduce power consumption and increase the bit-level with at least 16GSa/s sampling rate, which is the highest sampling rate reported so far in GaN technology to the best of our knowledge.

Asia-Pacific Microwave Conference (APMC) 2021

Mitsubishi Electric Research Laboratories, Inc.
201 Broadway, Cambridge, Massachusetts 02139

Full-Range Three-Stage 16GSa/s Riemann Pump RF-Power DAC in GaN HEMT

Tomoyuki Furuichi[‡#], Rui Ma[‡], Toshiaki Koike-Akino[‡], and Yuji Komatsuzaki[*]
[‡]Mitsubishi Electric Research Laboratories (MERL), Cambridge, MA, USA.
[#]Research Institute of Electrical Communication, Tohoku University, Sendai, Japan.
[*]Mitsubishi Electric Corporation, Information Technology R&D Center, Kanagawa, Japan.
Email: rma@merl.com

***Abstract*—In this study, we proposed a new encoding method to reduce power consumption and expanding the bit resolution of Riemann Pump (RP) digital-to-analog converters (DAC). In addition, a new circuit topology was demonstrated enabling high-side and low-side GaN transistors to operate independently such that the power consumption is significantly reduced by preventing unnecessary current flow. Moreover, our design realizes higher bit-level compared with the state-of-the-art complementary encoding method. We designed and fabricated a 3.9-bit RP using 0.15μm GaN process to validate its performance benefit. The simulation with practical device models confirms that our design can reduce power consumption and increase the bit-level with at least 16GSa/s sampling rate, which is the highest sampling rate reported so far in GaN technology to the best of our knowledge.**

***Index Terms*—Digital-to-analog converter, GaN, digital RF, transmitter architecture, low power consumption, fabrication**

I. Introduction

To support agile radio operation, software-defined radios (SDR) are investigated to push digital domain further towards antenna. Accordingly, an RF power digital-to-analog converter (DAC) which generates RF signals directly from digital front end is desired to reduce the counts of analog components such as mixers and local oscillators [1].

Recently, Riemann pump (RP) was proposed as a new type of RF-power DAC [1]–[6]. Connected with a power amplifier (PA) directly, it can synthesize nearly arbitrarily RF waveforms based on digital control words. The RP consists of multiple current-sources and switches to control current flow towards the input of the PA. The RP in [2] employs a complementary metal-oxide semiconductor (CMOS) technology using both p-type and n-type MOS (PMOS and NMOS) for high-side and low-side transistors, respectively. However, there is a drawback in multi-bit RP with the existing encoding pattern, where power is dissipated due to unnecessary current flows for certain required power levels (explained in details in section III).

In this paper, a mulit-bit RP is designed and evaluated using GaN HEMT process, which is an excellent wideband device technology offering much higher output power compared with CMOS. We propose a new encoding pattern to reduce power consumption and expanding the bit resolution. It realizes higher bit-level compared with complementary encoding patterns at 16GSa/s sampling rate. In following sections, encoding pattern, GaN RP design and performance will be provided.

II. Riemann Pump (RP) Basics

Fig. 1 shows the concept of the RP power DAC [2], which is based on binary-weighted current sources that pump charges to input capacitance of the PA. The current sources are controlled by switches, according to the desired voltage slope. Since the voltage is expressed as $v_{\rm out} = \frac{1}{C_{\rm out}} \int_0^t i_{\rm out}(\tau) {\rm d}\tau$, the RP can thus control the voltage slope by switching different current sources. The resolution of voltage slope depends on the number of stages of the current sources and current capabilities. In principle, the RP can generate high speed arbitrary RF waveform directly controlled by the output of DSP unit as shown in Fig. 1, manifesting itself a suitable power DAC for applications of SDR [2]–[6].

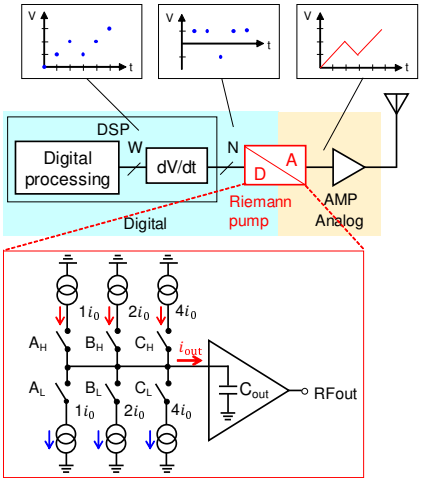

Fig. 1. 3-stage RP [2] for RF-power DAC.

III. Proposed Encoding Patterns for Improved RP

Conventionally, the high-side and low-side transistors are operated complementary in CMOS process. For example, a 3-stage RP in Fig. 1 has a 3-bit resolution to realize 2^3 possible currents, $i_{\rm out} \in \{\pm1, \pm3, \pm5, \pm7\} i_0$ for such CMOS operations (e.g., A_H and A_L are complementary ON/OFF). However, this CMOS encoding causes undesired current flowing to GND except the case of $i_{\rm out} = \pm7$, because at least one of high-side and low-side transistors have to be ON at the same time. For instance, to generate $i_{\rm out}$ =+5, A_L has to be

TABLE I
PROPOSED 3-STAGE RP ENCODING TABLE

Current	Hi-side			Lo-side		
i_{out}	A_H	B_H	C_H	A_L	B_L	C_L
$+7i_0$	1	1	1	0	0	0
$+6i_0$	0	1	1	0	0	0
$+5i_0$	1	0	1	0	0	0
$+4i_0$	0	0	1	0	0	0
$+3i_0$	1	1	0	0	0	0
$+2i_0$	0	1	0	0	0	0
$+1i_0$	1	0	0	0	0	0
$+0i_0$	0	0	0	0	0	0
$-1i_0$	0	0	0	1	0	0
$-2i_0$	0	0	0	0	1	0
$-3i_0$	0	0	0	1	1	0
$-4i_0$	0	0	0	0	0	1
$-5i_0$	0	0	0	1	0	1
$-6i_0$	0	0	0	0	1	1
$-7i_0$	0	0	0	1	1	1

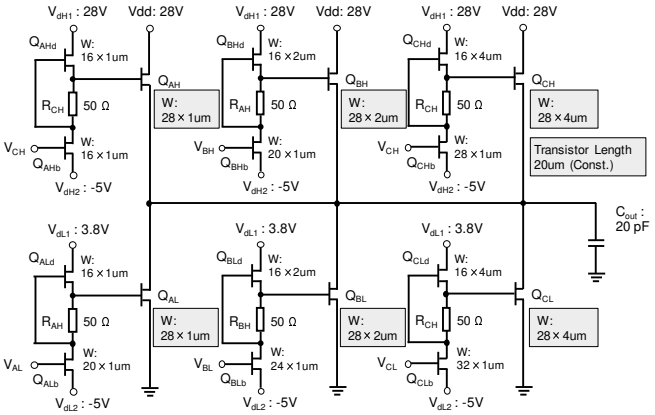

Fig. 2. Schematic of 3-stage RP.

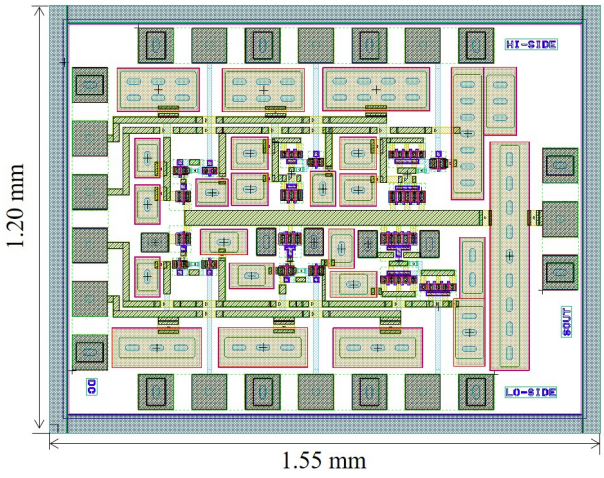

Fig. 3. Chip layout of 3-stage RP.

ON, in addition to B_H and C_H be ON. As a result, it leads to a waste of power, since i_0 is following to A_L too. Similarly, this applies for the other power levels as well.

Table I shows our proposed encoding patterns for RP modified for GaN process (considering only the widely available n-channel GaN HEMT device here only, not p-channel), where the high- and low-side transistors are allowed to operate independently. When the input is positive voltage slope, all low-side transistors are turned off, while all high-side ones are OFF for negative voltage slopes. Hence, the current all flows from/to the input capacitance without wasting. It can significantly reduce the driver power consumption. Moreover, since the high-/low-side translators are controlled independently, the RP bit patterns increased 8 (3-bit) to 15 (3.9-bit) levels compared with the complementary control pattern [1], without increasing the transistor stages as shown in Table I.

IV. 3-STAGE RF-DAC DESIGN

The signal-to-noise ratio (SNR) in dB is given as follows:

$$\text{SNR}_{\text{dB}} \approx 6.02N + 9.03\,r - 7.78 + 10\log\left(1 - \frac{1}{2^{N-1}} + \frac{1}{2^N}\right), \tag{1}$$

where N is the number of bits, and r is the binary logarithm of the over-sampling ratio (OSR). Specifically, we have $\text{OSR} = \frac{f_\text{S}}{2f_{\max}} = 2^r$ where f_S is the sampling frequency, and $f_{\max}$ is the maximum output frequency. More detail derivations are found in [3]. By comparison with pulse code modulation (PCM) conversion, the SNR of the RP is better than PCM conversion under the condition of $r > 2$ or $r > 1$ and $N > 2$. In this work, we focus on $N = 3.9$ and $r = 2$. For a target fundamental frequency of 2 GHz, $f_\text{S} > 16\text{GSa/s}$ is required ($\text{OSR} = 4$). Hence, an SNR of 33 dB is expected from (1).

We designed the 3-stage RF power DAC based on RP architecture shown in Fig. 1. The designed schematic is depicted in Fig. 2. We designed the core transistor size ratio to be Q_{AH}: Q_{BH}: Q_{CH}, Q_{AL}: Q_{BL}: $Q_{\text{CL}} = 1 : 2 : 4$, and output capacitor C_{out} is assumed 20 pF which is equivalent to the input impedance of the PA in [3]. The use of GaN technology restricts the inverter driver to non-complementary transistors, since p-channel GaN HEMT is not widely available. For the digital switching of the GaN power transistors, a switch-mode monolithic microwave-integrated circuit (MMIC) is used, having an implemented DTDR (depletion transistor, depletion and resistive load) driver circuit [3]. The DTDR driver consists of an interconnected depletion-mode transistor and resistive load. It enables both decreased static losses in the driver itself and improved switching characteristic, as mentioned in [7].

In multi-stage RP, it is important to match switching time (rising and falling) of each core transistor because its mismatch leads to distortion of the output voltage. To match the switching time of each core transistor, we optimized DTDR driver transistor size ratio to Q_{AHd}: Q_{BHd}: $Q_{\text{CHd}} = 1 : 2 : 4$. According to the proposed encoding table in Table I, each transistor is controlled interdependently. Our designed MMIC layout is shown in Fig. 3. Its fabrication in 150 nm GaN HEMT technology(f_t = 50 GHz,f_{max} = 246 GHz) is under the process.

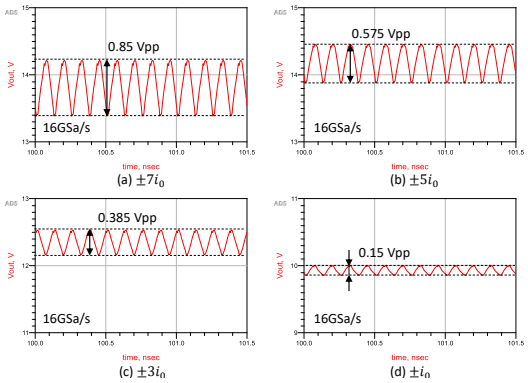

Fig. 4. 3-stage RP output voltage waveform (at 16 GSa/s).

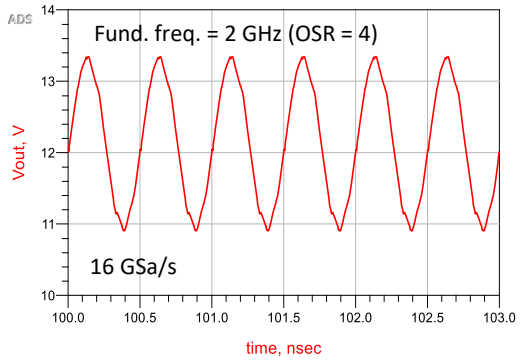

Fig. 5. Voltage waveform of the generated CW 2 GHz at 16 GSa/s.

V. Performance Results

We performed harmonic-balance, transient and layout simulations with practical devices non-linear large-signal models including parasitic effects. The simulated output voltage waveforms (ideally triangle wave) for constant current source at 16 GSa/s is shown in Fig. 4. It can be seen that the output voltage is controlled by each input bit pattern ($\pm 7i_0$, $\pm 5i_0$, $\pm 3i_0$, $\pm i_0$), functioning at 16 GSa/s. The simulated voltage waveform of continuous wave (CW) with a frequency of 2 GHz at 16 GSa/s is also shown in Fig. 5, with spectrum in Fig. 6. It can generate the fundamental frequency 2 GHz CW signal at the 16 GSa/s (OSR $= 4$).

Based on the above results, it was confirmed that the designed RP circuit achieves the target specification in the simulation. The summary of this work in comparison with the previous work [6] is listed in Table II, showing the improved performance in our design for both SNR and speed.

VI. Conclusions

We designed a new 3-stage RP using the GaN process to validate the advantage over the existing method. The primilary simulation results show a promising performance of the proposed design at high sampling rate of 16 GS/s. Therefore, RP based on GaN with enhanced coding schemes can be a viable candidate for the future digital transmitter in 5G and beyond. We will report experimental results of our RP GaN chip designed for fabrication in the near future.

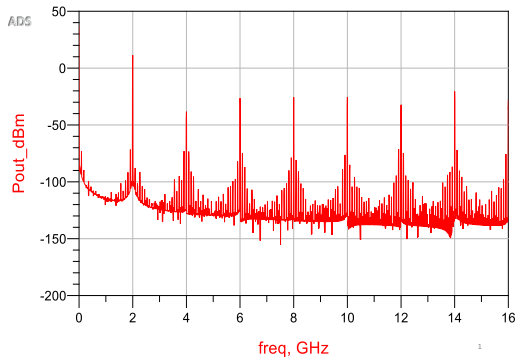

Fig. 6. Power Spectrum of the generated CW 2 GHz at 16 GSa/s.

TABLE II
Comparative Summary

Item	[6]	This work
Architecture	RP	RP
Technology	250nm GaN	150nm GaN
Resolution (bit)	2	3.9
Fundamental frequency	2 GHz (CW)	2 GHz (CW)
Sampling rate	8 GSa/s	16 GSa/s
Expected SNR	12 dB	33 dB

Acknowledgment

T. Furuichi was supported in part by the WISE Program for AI Electronics, Tohoku University.

References

[1] Y. Veyrac, F. Rivet, Y. Deval, D. Dallet, P. Garrec, and R. Montigny, "The Riemann pump: A concurrent transmitter in GaN technology," IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille, pp. 594–597, 2014.

[2] Y. Veyrac, F. Rivet, and Y. Deval, "Experimental demonstration of a Riemann pump RF-DAC in 65 nm CMOS," IEEE International Conference on Electronics, Circuits and Systems (ICECS), Monte Carlo, pp. 241–244, 2016.

[3] M. Weiß, C. Friesicke, T. Metzger, E. Schmidhammer, R. Quay, and O. Ambacher, "Design, realization, and evaluation of a Riemann pump in GaN technology," IEEE Microwave and Wireless Components Letters, vol. 27, no. 7, pp. 672–674, July 2017.

[4] F. Rivet, Y. Veyrac, and Y. Deval, "The Riemann pump: A technique For carrier-aggregation radio-frequency transceivers," IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Beijing, China, pp. 11–14, 2018.

[5] M. Weiß, C. Friesicke, R. Quay, and O. Ambacher, "Riemann-pump based RF-Power DACs in GaN technology for 5G base stations," IEEE MTT-S International Microwave Workshop Series on 5G Hardware and System Technologies (IMWS-5G), Dublin, pp. 1–3, 2018.

[6] M. Weiß, C. Friesicke, R. Quay, and O. Ambacher, "Integrated 2-b Riemann pump RF-DAC in GaN technology for 5G base stations," IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, pp. 1426–1429, 2019.

[7] S. Maroldt, C. Haupt, R. Kiefer, W. Bronner, S. Mueller, W. Benz, R. Quay, and O. Ambacher, "High efficiency digital GaN MMIC power amplifiers for future switch-mode based mobile communication systems," Annual IEEE Compound Semiconductor Integrated Circuit Symposium, Greensboro, NC, pp. 1–4, 2009.