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Abstract

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***Abstract*— This paper presents a fully-integrated two-stage GaN Doherty Power Amplifier (DPA) Module for 5G massive MIMO base stations. To overcome the size limitation of PAs in massive MIMO base-stations while meeting the wideband requirement, a new compact frequency-dependent compensating circuit with zero-phase offset in the peaking amplifier is proposed. The proposed circuit not only increases the bandwidth of the DPA, but also works as matching network, resulting in compact and flexible design. The proposed method is applied to a 10mm×6mm two-stage GaN DPA module. Measurements show that the DPA module achieves more than 50.4% drain efficiency and 42.9% PAE over 400MHz for 3.4-3.8GHz with -50dBc ACLR under 20MHz signal with PAPR of 8.0dB, after DPD. Furthermore, for 10 carrier aggregated signal (10×20MHz), the DPA exhibited 43.9% PAE with -48.6dBc ACLR after DPD. The proposed DPA has efficiency comparable to DPAs with larger sizes, demonstrating size advantage of the proposed configuration.**

***Keywords*— GaN HEMT, Doherty Power Amplifier, Carrier Aggregation, 5G, Digital Pre-Distortion, massive MIMO.**

I. Introduction

Wireless communication industry has been moving towards "5G", employing the massive MIMO antennas in base stations to meet the strong demand for high data rate and high connection density. In such a system, RF transceiver circuits are placed in the proximity of each antenna in the limited space between antennas. Thus the power amplifiers (PAs) in the transceiver circuits need to be much more compact than PAs in the "4G" technology [1]. Moreover, in order to realize high data rate, modulation signals with large peak to average power ratio (PAPR) and multiple Carrier Aggregation (CA) are necessary. Therefore, power amplifiers in "5G" technology are required to be efficient at a larger backed-off power level from saturation, and wideband without an increase in size.

To address those challenges, the Doherty Power Amplifier (DPA) using GaN is a good candidate due to superior material properties of GaN, and its relative simple efficiency enhancement technique of the DPA. In spite of the superior material properties which leads to compact, wideband and efficiency PAs, the DPAs are inherently narrow band and occupy large area due to a quarter-wave (λ/4) inverter required for the load modulation. Several papers [2][3] already show that it is possible to increase the bandwidth of DPAs by adding to the load end of the peaking amplifier the transmission line whose effective electric wave-length is integer multiple of half-wave (λ/2) [2][3], which we call as frequency-dependent compensation circuit (FDCC). However, this technique increases the size of DPAs, and is not applicable for PAs in massive MIMO base stations. In an effort to realize such a wide band DPA in a compact size, Jang et. al, [4] introduced DPA with zero-phase offset peaking amplifier. While this technique can increase the operating bandwidth of DPA without increasing in size, the transformed impedance of the peaking amplifier is limited, resulting in less design flexibility.

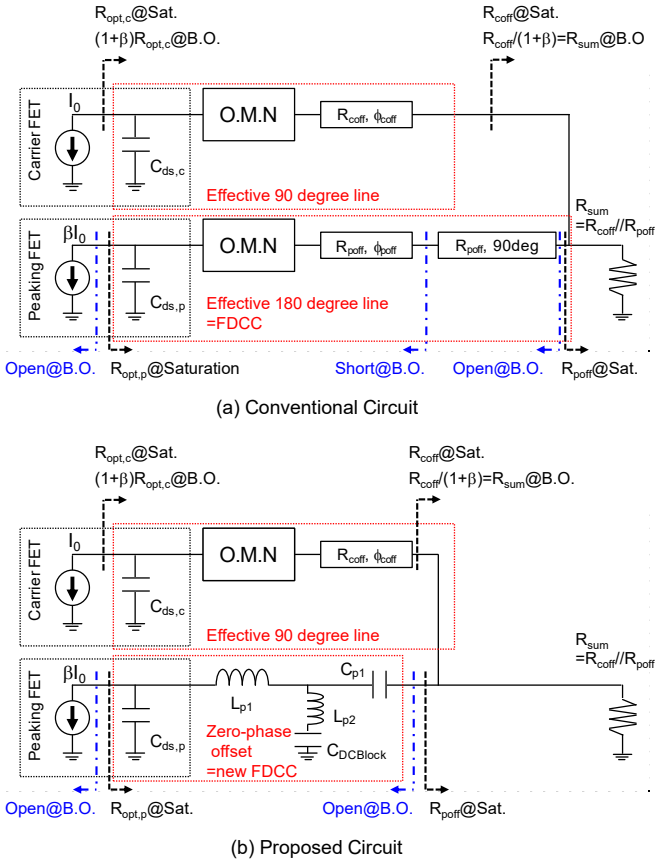

Fig. 1. Circuit diagram (a) the conventional DPAs and (b) proposed DPA.

In this paper, we present the design and characterization of a compact and fully-integrated two-stage GaN DPA with using a new FDCC circuit with zero-phase offset in the peaking amplifier. The proposed circuit not only increases the operating bandwidth but also works as matching network, resulting in a compact and flexible design. The proposed method is applied to a 10mm×6mm two-stage GaN DPA module. Measurement was done with using 20MHz and carrier aggregated signal (10 ×20MHz) with PAPR of 8.0dB. The measurement results will be shown and also compared with the state-of-the-arts results.

II. Circuit Design

A. Compact Frequency-Dependent Compensation Circuit

Figure 1 shows the circuit diagram of the conventional DPAs with FDCC and proposed DPA with a new compact FDCC. Since there exists parasitic components in FETs and dominant one is the source-to-drain capacitance, $C_{ds,c}$ and $C_{ds,p}$, the optimal impedances for carrier and peaking amplifier, $R_{opt,c}$ and $R_{opt,p}$, needs to be transformed by the output matching networks (O.M.N) to R_{coff} and $R_{poff,}$ respectively as shown in the figure. In the load end of the O.M.N, the offset lines are added to form effective quarter wavelength line for carrier amplifier and effective half wavelength line for the peaking amplifier in the conventional DPAs. In power back-off, peaking amplifier is completely off, and the effective half wavelength line works as open stub. This open stub becomes open at center frequency, and has capacitive impedance at higher frequency, and inductive impedance at lower frequency at the power combining node. This characteristic compensates the frequency dependence of the effective quarter wavelength lines in the carrier amplifier, resulting in the wideband operation of DPAs, as reported in [2][3]. In our proposed DPA, O.M.N and offset lines in peaking amplifier can be removed, and almost same electrical properties can be obtained by using series inductor, L_{p1}, shunt inductor L_{p2}, and series capacitor C_{p1}, as shown in Fig.1.(b). The circuit of the carrier amplifier is the same as that of the conventional one. The circuit which exchanges the position of L_{p2} and C_{p1} is reported in [4], where the impedance cannot be transformed and limited to the original value, $R_{opt,p}$, leading to limited design flexibility. In our proposed circuit, it is feasible to meet the requirement for FDCC and matching network simultaneously. The circuit parameters to meet those requirements are derived analytically as in the following equations,

$$\omega_0 L_{p1} = \frac{Q_{FET} - Q_1}{1 + Q_{FET}^2} R_{opt,p} \quad (1)$$

$$\omega_0 L_{p2} = \frac{\gamma_1}{Q_1 + Q_2} R_{opt,p} \quad (2)$$

$$\omega_0 C_{p1} = \frac{1}{\gamma_2 Q_2 R_{optp}} \quad (3)$$

,where $Q_{FET} = \omega_0 R_{opt,p} C_{ds,p}$, $\gamma_2 = R_{poff}/R_{opt,p}$. Here Q_1, Q_2 and γ_1 can be obtained by using Q_{FET} and γ_2 as follows,

$$Q_1 = \frac{-1 + \sqrt{\gamma_2}(1 + Q_{FET}^2)}{Q_{FET}} \quad (4)$$

$$Q_2 = \frac{Q_{FET} - Q_1}{1 + Q_{FET} Q_1} \quad (5)$$

$$\gamma_1 = \frac{1 + Q_1^2}{1 + Q_{FET}^2} \quad (6)$$

Therefore, once the optimal impedance, $R_{opt,p}$, and parasitic capacitance, $C_{ds,p}$, are extracted from the load-pull data, and impedance transformation ratio, γ_2, is determined, the circuit component in the peaking amplifier is uniquely derived from equation (1)-(6). Figure 2 shows simulated results of the impedance looking into peaking amplifier from the power combining node at saturation, $\Gamma_{p,sat}$, and power back-off, $\Gamma_{p,B.O.}$ with various impedance transformation ratio, γ_2. Circuit diagram to calculate the impedances are described in Fig.2. (a) and (b). As can be seen from the figure, the optimal impedance, $\Gamma_{p,sat}$, can be transformed into any real impedance lower than $R_{opt,p}$ at saturation, while the impedance at power back-off, $\Gamma_{p,B.O}$, has the frequency characteristic almost same as the conventional FDCC formed by half wavelength line, i.e. open at center frequency, capacitive at lower frequency and inductive at higher frequency. Therefore, by using the compact FDCC, it is possible to design wideband DPA without increasing in size and with flexibility in the impedance matching.

Based on the theory described above, the output combiner circuit was designed for the fully-integrated GaN DPA module as in the over-all circuit diagram shown in Figure 3. The gate peripheries of the carrier and peaking FETs were 2.4mm and 4.0mm, respectively. Thus asymmetry ratio, β, is 1.67. The impedance transformation ratio, γ_2, for both carrier and peaking amplifiers is set to 0.7 after trading off between the circuit loss and efficiency in the targeted bandwidth. The bonding wires connecting the FET and the circuit are included in L_{p1} in peaking amplifier. In the carrier amplifier, O.M.N is formed by series bonding wire L_{c1}, shunt inductance L_{c2}, and the offset line is formed by the transmission line, TL_{c1}, as shown in Fig. 3.

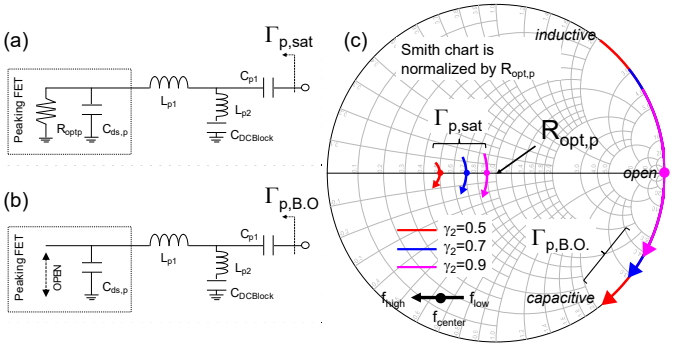

Fig. 2. Simulated results of the impedance looking into peaking amplifier from the power combining node at saturation, $\Gamma_{p,sat}$, and power back-off, $\Gamma_{p,B.O}$ with various impedance transformation ratio, γ_2.

B. Input Network and Driver stage

The circuit diagram of the input network and configuration of the driver stage are described in Figure 3. In order to minimize the size of the module, all the components in the input network of the DPA are realized by GaAs MMICs or Surface Mounted Devices (SMDs). GaAs MMICs are placed in the vicinity of the FETs, and include the stability network and part of the input matching network. The phase offset line for the input of the peaking amplifier is formed by pi-network, and in the similar

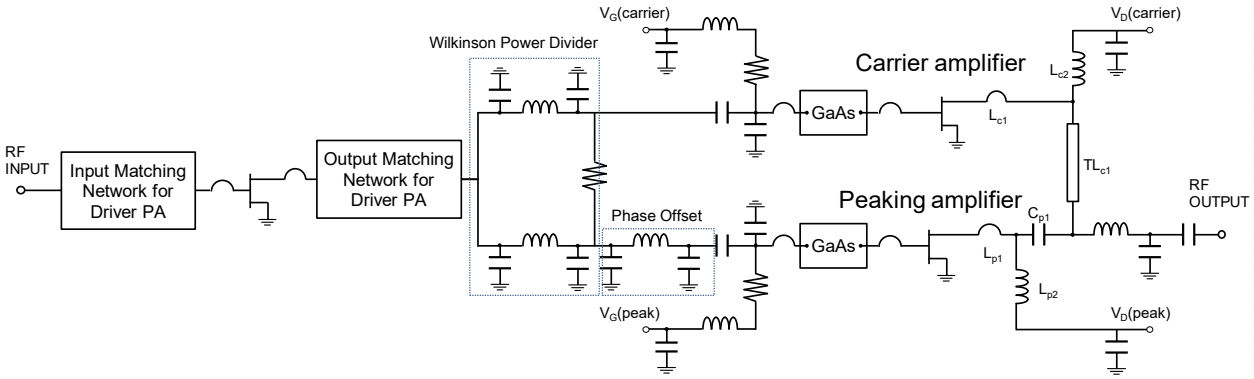

Fig. 3. Circuit diagram of the fully-integrated two-stage GaN Doherty Power Amplifier (DPA) Module with a compact FDCC circuit in the peaking amplifier.

way, the quarter wavelength lines for the Wilkinson power divider are also formed by pi-networks. Driver stage PA is connected to the input of the Wilkinson power divider. Both output matching network and input matching network for the driver stage are also designed using SMDs for a compact design. All those component are integrated in the 10mm × 6mm multilayer epoxy substrate and molded from the top.

III. Implementation And Measurement Results

Figure 4 shows the photo of the fully-integrated 2-stage GaN DPA module with the compact FDCC before and after molding. For carrier and peaking amplifier, Mitsubishi Electric's GaN HEMTs are used. The molded module was implemented on an evaluation board (EVB) with 50Ω input and output line and bias feed line. The loss of the 50Ω lines on the EVB are de-embedded from EVB measurements and all the measurement results are at module reference planes. In our measurement, all the drain voltage was set at 39V, and the main amplifier and driver amplifier were biased at Class-AB, and the peaking amplifier was biased at Class-C. Figure 5 shows the measured drain efficiency for the final stage DPA (DE(final)), Power

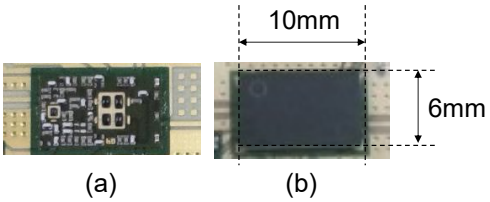

Fig. 4. Photo of the fully-integrated 2-stage GaN DPA Module with a Compact FDCC (a) before molding and (b) after molding.

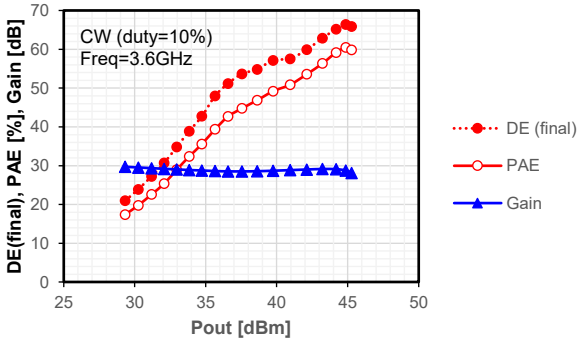

Fig. 5. Measured drain efficiency for the final stage and power added efficiency and gain for 2-stage PA under 3.6GHz continuous wave signal.

Added Efficiency (PAE) which include the power consumption of driver stage and Gain for 2-stage PA under 3.6 GHz continuous wave (CW) signal. Load modulation of the DPA is clearly observed with a peak output power of 45.3 dBm. DE(final) of 53.7% and PAE of 44.8 % at the 8 dB output power back-off level is obtained.

Figure 6 shows the measured PAE, Gain and adjacent channel leakage ratio (ACLR) at 3.5GHz using 20MHz modulated signal with PAPR of 8.0dB w/ and w/o Digital Pre-Distortion (DPD). As shown in Fig. 6 the proposed GaN DPA module achieves the maximum PAE of 47.8% with ACLR of -50dBc. The measured frequency characteristic using the same 20MHz signal are shown in Fig. 7. Maximum PAE, DE for final stage, Gain and output power (Pout) at ACLR of -50dBc w/ DPD is plotted as a function of frequency. Over the 3.4-3.8GHz frequency band, the proposed DPA obtains the PAE of 42.9-47.8%, DE for final stage of 50.4-54.8%, Gain of 26.9-28.6dB, and Pout of 37.7-38.5dBm.

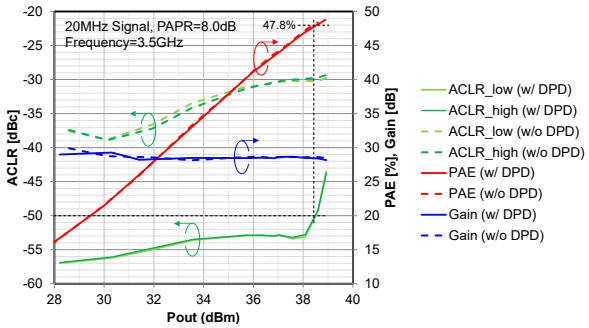

Fig. 6. Measured PAE and Gain and ACLR at 3.5GHz using 20MHz modulation signal with PAPR of 8.0 dB.

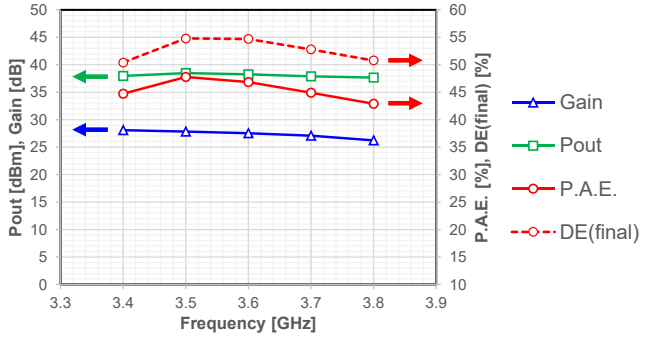

Fig. 7. The measured frequency characteristics using the same 20MHz modulation signal with PAPR of 8.0dB.

Table 1. A Performance comparison of the proposed DPA with the state-of-the-art DPA for 3-4GHz band.

Ref	Year	Freq [GHz]	Size [mm*mm]	DE(final) [%]	PAE [%]	Pout [dBm]	Gain [dB]	ACLR [dBc]	Mod. BW [MHz]	PAPR or B.O. [dB]
[5]	2012	3.0-3.6	*1	38-54			8-11		CW	6
[6]	2013	3.45	*1	42.5		40.4		-48	100	8.5
[7]	2016	3.5	100mm*95mm	58	52	36.5	8	-52	20	9
	2016	3.5	100mm*95mm	56	51	36.5	8	-50	100	9.7
[8]	2016	3.3	*1	43.4		39.1		-47.8	20	7.2
[9]	2017	3.5	*1		55	33.9	9		CW	9
[2]	2017	3.0-3.6	78mm*60mm	45.9-50.2		34.1-34.6		-50	20	7.5
[10]	2019	3.5	*1	35.7	29.3	33	7.5-11.7	-50.7	200	7.7
[11]	2019	2.55-3.8	*1	47-60		40.8-41.8	9.3-12.7		CW	8
		3.2	*1	51		40.5		-50	140	8
This Work	2020	3.4-3.8	10mm*6mm	50.4-54.8	42.9-47.8	37.7-38.5	26.9-28.6	-50	20	8

*1 Sizes are not written in the paper, but they are designed on PCB and have much larger size than 10mm×6mm

A performance comparison of the proposed DPA with the state-of-the-art DPA for 3-4GHz band is shown in Table 1. In spite of few reports on DPA with similar size, our proposed DPA achieved comparable efficiency to DPAs with much larger sizes. Size advantage of the proposed configuration is clearly demonstrated, which is strongly required in 5G massive MIMO applications.

To further demonstrate the wideband characteristic, measurements with using multi-carrier aggregated (CA) signal were also performed. Figure 8 shows the measured spectra with DPD at 3.6GHz under 10 CA signal (10×20MHz) with PAPR of 8dB, demonstrating that the designed DPA can be linearized even under wideband modulation signals. Measured results with multi-CA signals are PAE of 43.9% at Pout of 38dBm with ACLR of -48.6dBc.

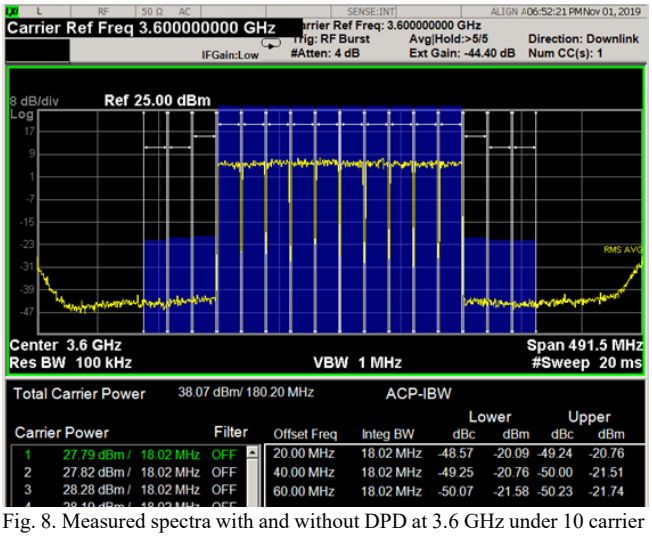

Fig. 8. Measured spectra with and without DPD at 3.6 GHz under 10 carrier aggregated LTE signal (10×20MHz).

IV. Conclusion

To realize the compact and wideband DPA for 5G massive MIMO applications, the new compact FDCC were proposed. The developed fully-integrated GaN DPA module has comparable efficiency with DPAs with much larger sizes. The wideband characteristic is verified by the measurements using multi-carrier signals up to 200MHz. In addition the proposed DPA exhibits high efficiency over 400MHz for 3.4-3.8GHz range which covers most of 5G bands in sub-6GHz.

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