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Abstract

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JLT (Invited Review Paper)

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Miniaturized silicon photonics devices for integrated optical signal processors

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(Invited Tutorial)

Abstract—Integrated optical signal processors, in combination with conventional electrical signal processors, are envisioned to open a path to a new generation of signal processing hardware platform that allows for significant improvement in processing bandwidth, latency, and power efficiency. With its well-known features and potential, silicon photonics is considered as a favorable candidate for the device implementation, particularly with high circuit complexity, and hence has been the focus of the study. As an outlook from the previous discussions on such processors, we are considering new building blocks in the silicon photonics platform for further extending the processor capabilities and adding practical features, particularly the miniaturized devices that enable ultra-dense integration of complex circuits into such processor chips. As enlightening examples, we review here our recent contribution together with representative works from other groups of compact designs of silicon photonics devices that enrich functionalities of processor building blocks such as multiplexing, polarization handling, and optical I/Os. The results shown in this review reflect the significance and maturity of the state-of-the-art photonic fabrication technology and contribute to the implementation of high-capacity, general-purpose optical signal processing functionalities on the chip scale.

Index Terms—Silicon photonics, programmable photonics, optical signal processing, reversed design, lithium niobate modulator.

I. INTRODUCTION

IN recent decades, optical signal processing, as often compared with conventional and industry-mature digital signal processing technology, has made considerable strides in its essence and use, owing to its uniqueness of providing a combination of desirable features such as large bandwidth, low latency, high temporal resolution, efficient power consumption, and information security. Implementing optical signal processing functions in photonic integrated circuits (PICs) yields the so-called integrated optical signal processor (IOSP) chips [1, 2], which open a path to a new generation of signal processing hardware platform that supports the combination of

microelectronics and photonics, thereby provides signal processing capabilities beyond electronics-only approaches. Such optical signal processor chips are expected to be of great use in many technological areas, including Tbit/s-level telecom and datacom optical transceivers [3], capacity-multiplication of optical switches and reconfigurable optical add-drop multiplexers (ROADMs) [4], optical sensor networks for Internet of Things (IoT) [5] and self-driving automotive [6], radio-frequency photonics in defense and 5G wireless communications [7, 8], quantum computing [9], and photonic artificial intelligence (AI) [10].

As an interesting study for increasing the application range and cost efficiency per chip, some recent works aimed at general-purpose processor chips which incorporate on-chip functional programmability using a reconfigurable mesh network circuit architectural concept like that of microelectronic field-programmable gate arrays (FPGAs) [11–16]. Figure 1 shows designs of such chips with three different mesh architectures, where Mach-Zehnder interferometers (MZIs) serve as tunable basic units (TBUs) that compose couplers with two-inputs-two-outputs waveguides for the interconnections in the mesh network and perform independent control of amplitude and phase of light at coupler outputs using phase tuning elements in both arms [11]. The choice of the mesh

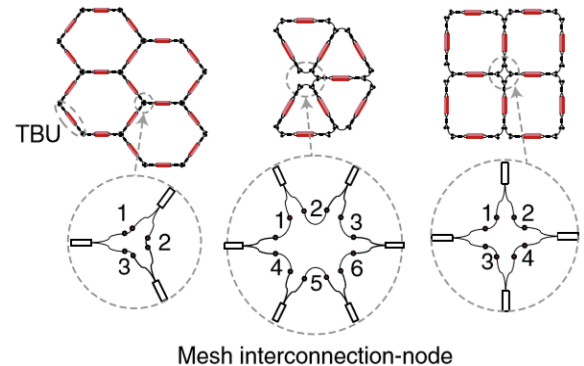


Fig. 1. Reconfigurable mesh designs of three different types: hexagonal, triangular, and square type, with illustrations of their associated interconnection points [17] (Copyright in 2016, OSA).

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architecture determines several figures of merit regarding circuit performance and layout reconfiguration [13]. An early demonstration of such a chip with two square cells showed its capability of implementing a Hilbert transformer, a delay line, and both notch and bandpass filters [11]. Another work demonstrated such a waveguide mesh composed of 7 hexagonal cells, capable of implementing over 100 different circuit layouts and functions [12].

To date, a number of material platforms have been explored for the implementation of IOSP chips [2], including silica, silicon-on-insulator (SOI), silicon nitride, GaAs, InP, AlN, LiNbO₃, chalcogenide glass, polymers, and organic as well as metallic materials, the choice of which determines processor functionality, performance, physical dimensions, and system complexity. However, as illustrated in Fig. 1, for the consideration of general-purpose processor chips that can be widely applied like microelectronic FPGAs, component size miniaturization and dense control deployment are strongly desired for the material platform in order to support high circuit complexity required by functional flexibility and scalability. Silicon photonics is therefore considered as a favorable candidate, not only for its features of high circuit compactness and well-developed design as well as fabrication environment, but also for its low-cost, large-scale integration and possibility for a wide range of device functionalities via hybrid integration with other photonic materials as well as electronics [18–20]. However, further efforts are needed to address practical issues on device footprint, loss, control, power consumption, and operation robustness against fabrication imperfections. For further advancement of this field, another consideration is to incorporate the frontiers in silicon photonics integration technologies, e.g., hybrid or heterogeneous integration [21], utilizing the broadened device capabilities to tackle new challenges in signal processing applications.

As previously demonstrated, most signal processing functions implemented in silicon waveguide mesh networks use passive interferometric circuitry that operates with signals on a single optical carrier [12]. With respect to this limitation, in this paper, we consider new building blocks in silicon photonics platform for further extending the processor capabilities and adding practical features, e.g., increasing processing capacity by enabling parallel processing of multiple signals for different

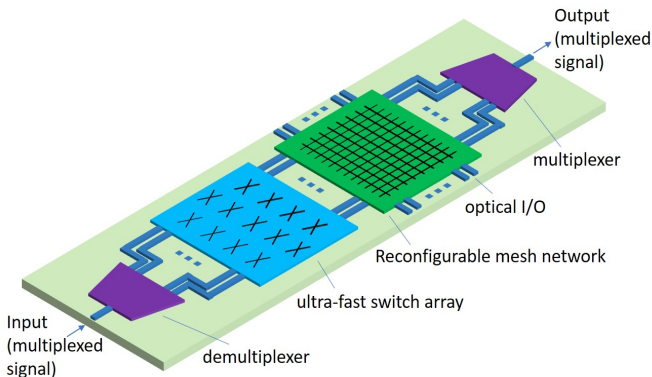


Fig. 2. Visionary drawing of a general-purpose integrated optical signal processor incorporating functionalities of signal (de)multiplexing, ultra-fast switch array, and reconfigurable mesh network in one platform.

multiplexing schemes, which are of particular interest for applications in telecommunications, data center communications, and ultra-fast computing. Figure 2 shows a visionary drawing of the IOSP architecture that combines new capabilities and a mesh network in one platform, where a scalable processing capacity is considered based on signal multiplexing schemes with optical carriers defined in terms of wavelength, mode, polarization, etc., depending on applications. Here, a dedicated demultiplexer splits multiple optical carriers into separate optical paths so that each can be processed later independently. The mesh network performs as a multiple-input-multiple-output (MIMO) system with a certain signal processing function implemented between each input-output pair. Before the mesh network, a building block as an ultra-fast (e.g., < 20 ps) switch array is desired that reconfigures the mapping between the separated optical carriers and the mesh network inputs (processing functions). Such a functionality overcomes the slow thermo-optical tuning mechanism that is preferred to use in the mesh network because of its small device size [12]. After being processed in the mesh network, each optical carrier can be routed to one of the optical I/Os or be multiplexed again into a common output, depending on the system requirement.

As enlightening examples for device implementation, we review our recent contribution and representative works of other groups of compact designs of silicon photonics devices that enrich functionalities of processor building blocks such as multiplexing, polarization handling and fiber-to-chip couplers as optical I/Os. The focus of this paper is passive functionalities for IOSP chips, while our future perspective also covers a discussion on heterogeneous integration of high-bandwidth electrooptical modulators, i.e., lithium niobate-on-insulator (LNOI) modulators [21], as a potential solution for the ultra-fast switch array. These building blocks also represent a great potential for high-throughput, fast computing functionalities in compact designs, which implies a new category of applications for IOSP chips, such as photonic AI and quantum computing.

II. MINIATURIZED PASSIVE SILICON DEVICES AS SIGNAL PROCESSOR CHIP BUILDING BLOCKS

Miniaturized photonic devices have been aggressively studied over recent years, with the aim of minimizing chip footprints while maintaining performance. Silicon photonic devices have made rapid progress to provide advanced functionalities and improved performance for a wide variety of optical signal processing tasks [22] such as wavelength division multiplexing (WDM), mode manipulation, polarization handling and fiber-to-chip coupling. These devices are of great interest for the implementation of IOSPs because miniaturized devices mean more complex circuits with more advanced functionalities per unit area. This might mean increased capacity of multiplexers, modulators and switches in the same footprint or the same capacity with reduced latency afforded by smaller footprints. Similarly, compact and efficient fiber-to-chip couplers are of great importance for optical I/O to large-scale IOSP chips.

In this section, we review several recent works of passive silicon devices with focus on demonstrations using

subwavelength components and inverse design approaches that support the miniaturization of device dimensions and provide additional benefits for the design process. An overview of these devices is given in Table 1. Unlike conventional design approaches using a combination of well-studied device physics and geometries, inverse design treats photonic structure as a “black box” and use optimization algorithms to reach certain geometries with desired performance [23]. Popular algorithms for topology optimization include particle swarm algorithm [24], adjoint method [23], direct binary search [25], etc., which have resulted in device designs with exceptionally small footprints.

A. Devices for Parallel Processing of Multiple Signals

Integrating WDMs for multiplexing/demultiplexing in IOSP chips enables parallel processing of multiple signals carried on different wavelengths. Typical implementations use arrayed waveguide grating (AWG) [26], echelle grating [27], or cascade of multiple double-bus ring resonators [28]; all of these utilize complex interferometric circuits and consume significant real estate on the chip. A recent study using inverse design based on topology optimization, however, has demonstrated a wavelength demultiplexer of 3 wavelengths on a footprint of $5.5 \mu\text{m} \times 4.5 \mu\text{m}$ [23] as shown in Fig. 3. In principle, the subwavelength structure can be further expanded to handle more wavelengths with lower crosstalk, providing capabilities comparable to AWGs and echelle gratings but with orders-of-magnitude size reduction.

Complementary to WDM techniques, on-chip mode manipulation is another important route to signal multiplexing via mode division multiplexing (MDM) [29]. MDM enables further capacity gains in IOSPs by enabling parallel processing on multiple signals carried on different waveguide modes. Driven by a variety of potential applications in optical communications and sensing, on-chip mode manipulation has made significant progress in the recent years with demonstration of essential functionalities including splitters [30, 31], sharp bends [32–34], waveguide crossings [35], channel filters [36] and converters [37] implemented for multi-mode operations. Beyond MDM, on-chip mode manipulation also finds use in polarization handling which is important for IOSP implementation and will be discussed further in subsection B. Recent works have shown promising results towards large-scale circuit implementation of ultra-compact MDM devices to support miniaturization of these key technologies.

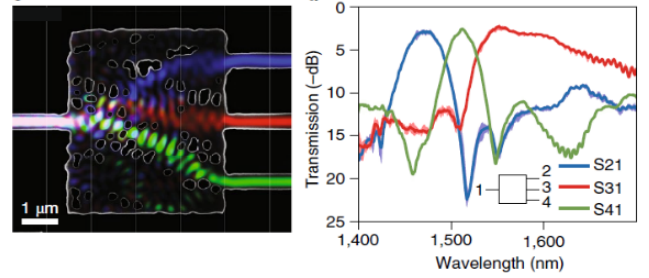


Fig. 3. Topology optimized three-wavelength demultiplexer and its measurement spectrum [23] (Copyright in 2018, Nature).

Consider a 90-degree bend as an elementary building block for on-chip routing; bends in conventional single-mode Si waveguides are compact with low insertion loss. However, a much larger bending radius is typically needed in a multimode waveguide to suppress modal crosstalk [29]. Figure 4 shows recent development of sharp multimode waveguide bends [32, 33] much smaller than those achievable using conventional waveguides. Sharp dual-mode waveguide bends were demonstrated using mode converters and subwavelength geometry, where minimal insertion loss and modal crosstalk can be maintained at the same time. Multimode waveguide bends supporting more than 2 eigenmodes have also been reported [29] but require larger bending radius.

Recently, two symmetric Y junctions were connected by ultra-sharp single-mode waveguide bends, as shown in Fig. 5. The dual-mode bend was designed at a central wavelength so that the two routes differ in phase by a multiple integer of 2π . Measurements show 1.2 dB insertion loss with less than -20 dB TE_1 crosstalk measured over 20 nm bandwidth. Similarly, dual-mode S bend can be easily designed, leading to colorless crosstalk suppression on flexible S bend geometries [34].

Compact multimode demultiplexer is another vital

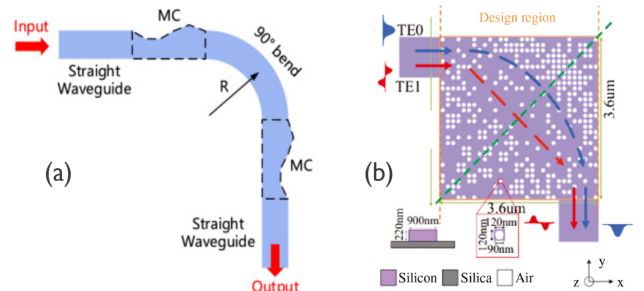


Fig. 4. Schematics of (a) a dual-mode sharp bend using mode converter [32] and (b) a dual-mode sharp bend using inverse design [33] (Copyright in 2017 & 2018, OSA).

TABLE I
LIST OF REPORTED WORKS ON COMPACT SUBWAVELENGTH DEVICE BASED ON INVERSE DESIGN

Published work	footprint	performance
Three-wavelength demultiplexer [23]	$5.5 \mu\text{m} \times 4.5 \mu\text{m}$	Less than 3dB loss and -10 dB crosstalk
Two-mode sharp bend [33]	$3.6 \mu\text{m}$ radius	0.8 dB insertion loss with -24 dB modal crosstalk
Three-mode demultiplexer [35]	$2.4 \mu\text{m} \times 3 \mu\text{m}$	1 dB insertion loss with -24 dB modal crosstalk over 80 nm bandwidth
Three-mode waveguide cross [35]	$34 \mu\text{m} \times 34 \mu\text{m}$	0.9 dB insertion loss with -24 dB modal crosstalk over 80 nm bandwidth
Mode converter [37, 38]	$3.85 \times 2.35 \mu\text{m}$	0.5 dB insertion loss with -15 dB modal crosstalk
Two-mode exchange [47]	$4 \mu\text{m} \times 1.6 \mu\text{m}$	2.5 dB insertion loss
Two-mode 3dB power splitter [27]	$2.88 \mu\text{m} \times 2.88 \mu\text{m}$	1.5 dB insertion loss with -20 dB modal crosstalk
PBS [59]	$2.14 \mu\text{m} \times 2.14 \mu\text{m}$	Average efficiency $\sim 70\%$ with 10 dB extinction ratio over 32 nm bandwidth
PR [60]	$5 \mu\text{m} \times 1.2 \mu\text{m}$	Average efficiency $\sim 37\%$ with 9 dB extinction ratio over 40 nm bandwidth
Grating coupler [71]	$12 \mu\text{m} \times 12 \mu\text{m}$	-3 dB coupling efficiency over 100 nm bandwidth

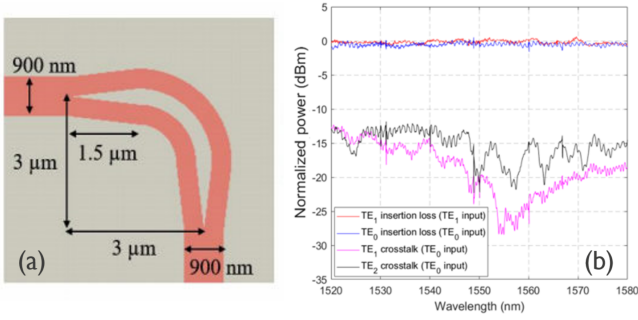


Fig. 5. (a) Layout of a 3- μm radius dual-mode bend using symmetric Y junctions [34] (Copyright in 2018, OSA). (b) Measurement spectrum of the 3- μm radius dual-mode bend [38].

component to miniaturize MDM circuit. The standard approach uses multiple asymmetric directional couplers (ADCs) [29] or ring resonators [39, 40] to (de)multiplex different waveguide modes one by one. Inverse design based on topology optimization [41] can generate compact subwavelength structure that demultiplexes three waveguide modes on one single device. Miniaturized waveguide mode demultiplexers can also be used to construct a multimode waveguide cross, where Fig. 6 shows an architecture to realize a three-mode cross [35].

Mode order conversion is another important aspect of mode manipulation and this can provide channel conversion for MDM systems. Mode converters can also be used to provide flexible power splitting [42] and polarization handling [43]. Figure 7 shows example mode converters with high efficiency based on compact structures such as adiabatic taper [44] and nano-trench structures [45].

Recently researchers have used compact subwavelength structure from inverse design to implement mode conversion [37], as shown in Fig. 8. One clear advantage of subwavelength mode converters is that different high order modes can be directly converted on a single compact device. For instance, TE_1 -to- TE_2 can be directly converted in a miniaturized subwavelength structure; in contrast, using low-loss tapers

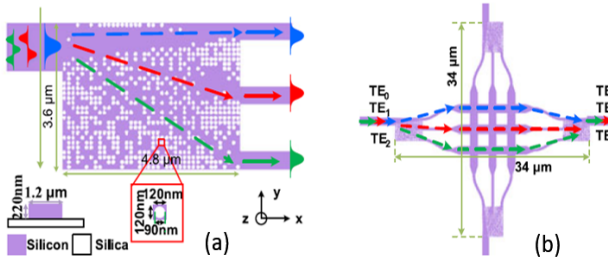


Fig. 6. (a) Compact subwavelength structure for three-mode demultiplexer [35] (Copyright in 2018, OSA), (b) schematic of a three-mode waveguide cross based on the compact three-mode demultiplexer [35] (Copyright in 2018, IEEE).

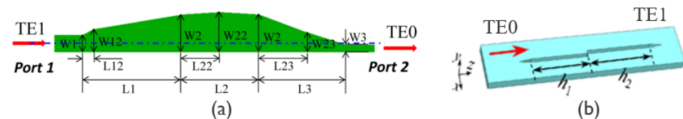


Fig. 7. Schematics of (a) a mode converter based on low-loss taper [45] (Copyright in 2015, OSA) and (b) a mode converter based on nano-trench [46] (Copyright in 2017, OSA).

requires two mode converters and use of an intermediate TE_0 mode. The design is experimentally validated by using ADCs to generate and detect high order modes, where most output power should be TE_2 mode. Experimental results show ~ 0.5 dB insertion loss and exceeding 15 dB modal crosstalk suppression over 100 nm bandwidth for such mode converter. Dimension sensitivity is also studied over various hole diameters around nominal sizes, and measurement shows hole diameter of ± 10 nm which leads to additional insertion loss of 1.5 dB [38].

Mode converters can be further extended to perform the functionality of mode exchange where different MDM modes exchange their signals between one another. Figure 9 shows two examples of such devices that are capable of swapping MDM signals between TE_0 mode and TE_1 mode [47, 48]. The device in Fig. 9(a) is based on Y junctions which allows the use of thermal phase shifter to control mode exchange.

Mode converters may also be used for mode switching. For example, a mode demultiplexer may utilize switching control to exchange signals at output ports. Figure 10 shows a high-speed two-mode switch [44] with reported switching time less than 2.5 ns using a PN phase shifter and 10 Gb/s input signals. Such dynamic mode control is important for the implementation of TBUs in IOSPs that support multi-mode operations. Considering the demonstrations on tunable mode exchange and mode switching, it is very likely that a conventional 2×2 switch can be tweaked to support multiple modes and yield TBUs with enhanced signal processing power.

Furthermore, multimode power splitters are also indispensable MDM devices. To enable a practical circuit to support multiple modes, a multimode power splitting scheme is paramount. Cascaded ADCs were introduced in Ref. [50], followed by more compact subwavelength dual-mode splitters

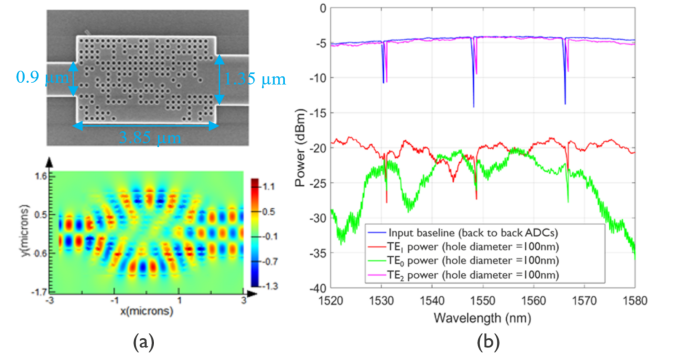


Fig. 8. (a) Photo and simulated field distribution of a TE_1 -to- TE_2 converter based on single compact subwavelength device [37] (Copyright in 2018, OSA). (b) Device spectrum measurement where high-Q ring resonance is maximized for pure TE polarization during edge coupling [38].

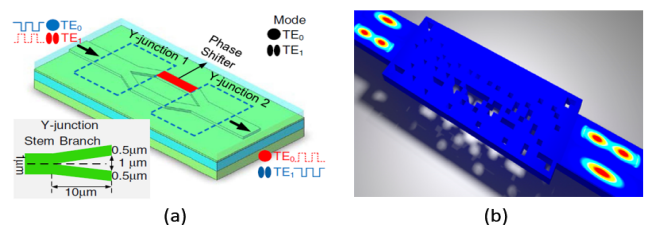


Fig. 9. Schematics of (a) a TE_0 -to- TE_1 mode exchange with thermal control [47] (Copyright in 2017, OSA) and (b) a passive TE_0 -to- TE_1 mode exchange based on compact subwavelength geometry [48] (Copyright in 2018, ACS).

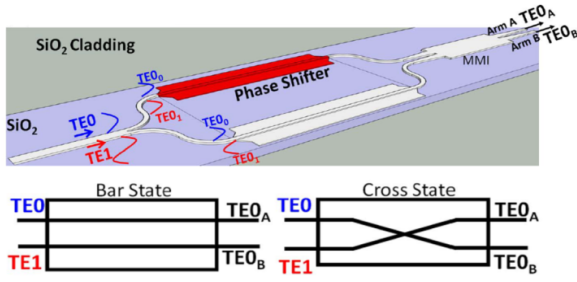


Fig. 10. Schematic of a high-speed two-mode switch and two states [49] (Copyright in 2018, OSA).

using inverse design in Fig. 11 (a) [31]. However, these devices cannot be easily scaled up due to insertion loss or footprint. Another practical bottleneck is presented by modal crosstalk, which leads to different power splitting ratios when input modes are at different relative phase (phase sensitivity).

Polarization rotation has been proposed to convert TE_1 to TM_0 while TE_0 remains unaffected [38]. Then TE_0/TM_0 will be equally divided by cascaded Y junctions with negligible loss and ultimately converted back to TE_0/TE_1 . With modal crosstalk annihilated before the Y junction, this dual-mode splitter becomes immune to phase sensitivity. This splitter architecture is easily scalable and a 1-to-8 splitter using this concept is shown in Fig. 11.

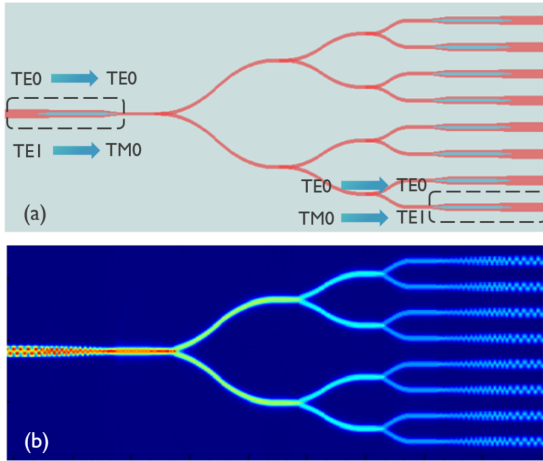


Fig. 11. (a) Schematic of a dual-mode 1-to-8 splitter using polarization rotation, (b) $|E|$ plot when both TE_0 and TE_1 are injected concurrently [38].

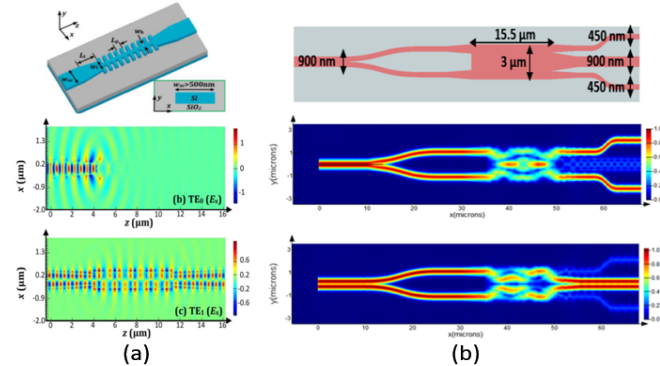


Fig. 12. Layout and simulated field distribution of (a) a TE_1 -pass- TE_0 -block filter based on Bragg reflector [51] (Copyright in 2015, OSA), (b) a TE_1 -pass- TE_0 -block filter based on MMI [52] (Copyright in 2019, OSA).

Finally, mode filtering is an important mode manipulation used to suppress undesired modal crosstalk. Getting rid of weakly confined high order modes is straightforward but to preserve high-order modes and dump the better confined low-order modes becomes a formidable challenge. Over recent years, high-order mode pass filters have been reported by using Bragg reflector [36] and mode exchange [51]. Bragg reflector can be designed such that one mode is designed within the Bragg reflection zone while another mode is assigned to subwavelength grating (SWG) waveguide propagation zone [36]. Alternative methods based on mode exchange [51] are also interesting wherein TE_0 is filtered by exchanging with radiative high-order modes. More recently a high order mode pass filter is reported based on MMI as shown in Fig. 12 [52]. Such mode filter cleanses TE_0 mode by radiation rather than reflection and meanwhile TE_1 power transmission is immune to modal crosstalk due to horizontal symmetry. Measurement shows < 1.5 dB TE_1 insertion loss with > 15 dB TE_0 filtering over C band [52].

B. Devices for Polarization Handling

Incorporating polarization management in IOSP chips is crucial for robust and efficient system architectures. From a practical perspective, most photonic devices have birefringence and polarization management is needed on chip when the processing function requires a specific polarization state while the input polarization state is typically unknown for many application scenarios. A common solution supports polarization diversity [53] by utilizing a polarization beam splitter (PBS) and polarization rotator (PR) to convert the input to a known polarization state. PBS and PR are also widely used for polarization division multiplexing (PDM), which doubles the data capacity at marginal cost. This subsection outlines recent progress in polarization handling devices to support inter-chip communication between optical processors.

On the SOI platform, PBS is usually implemented using an asymmetric directional coupler, which allows TM_0 to couple

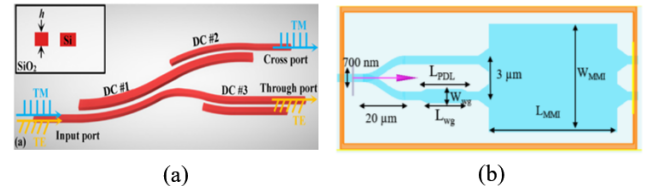


Fig. 13. (a) Schematic of a SOI PBS based on curved ADCs [54] (Copyright in 2017, OSA). (b) Layout of a SiN PBS based on MMI and phase delay line [55] (Copyright in 2017, OSA).

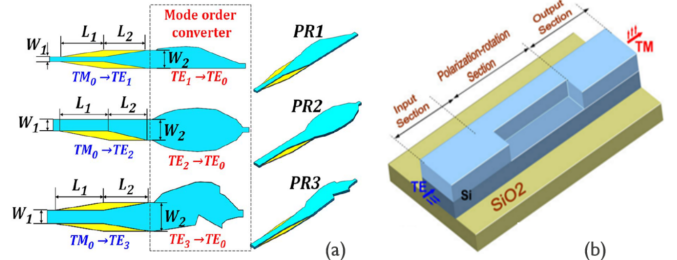


Fig. 14. Schematics of (a) a PR based on mode order conversion [56] (Copyright in 2016, OSA) and (b) a PR based on partially etched Si structure [58] (Copyright in 2014, Hindawi).

through while leaving the TE_0 unaffected. Figure 13 shows a recent demonstration of silicon photonic PBS, where multiple curved ADCs are used to separate TE and TM polarizations [54]. However, this technique does not work well in a low-birefringence platform such as SiN. Research has been reported using a 2×2 MMI and phase delay line to split polarizations in a single-layer SiN structure [55]. The design relies on a special phase delay line that gives one polarization pair $\pi/2$ phase shift and $-\pi/2$ phase shift for the other, which steers TE/TM to different output ports of MMI.

Polarization rotation is the functionality to convert between TE and TM mode. Unlike PBS, polarization rotation requires breaking vertical symmetry to enable hybrid polarization modes. This is typically accomplished using a different top cladding material (such as air, polymer, SiN) [56] or to partially etch Si layer [57, 58]. Figure 14 shows some reported PR designs based on partially etched SOI structures. For standard 220 nm Si thickness, TM_0 mode is first converted to high-order TE mode, which is converted back to TE_0 by mode order converter [44]. Other PR designs based on mode evolutions are also reported, which usually demands thicker Si layer thickness [58]. Miniaturization of PBS and PR using inverse design have also been reported [59, 60], as illustrated in Fig. 15. With air-cladded digital metamaterial structure, silicon photonic PBS and PR can be demonstrated in an ultra-compact footprint.

Further combination of PBS and PR leads to polarization splitter and rotator (PSR), which is widely used for polarization diversity schemes. Compact PSR device ($< 50 \mu\text{m}$ long) on air cladded SOI platform has been reported based on multimode waveguide, as shown in Fig.16 [61]. Theoretically PSR needs to be long enough to suppress polarization crosstalk at output ports. This work deploys a curved directional coupler to filter the crosstalk power, enabling extinction ratio exceeding 20 dB

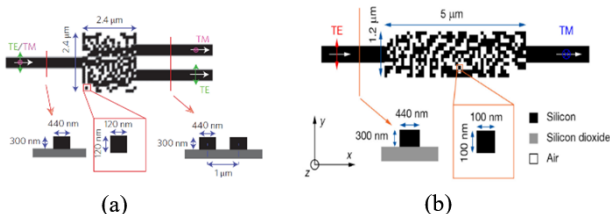


Fig. 15. Layouts of (a) a digital dielectric metamaterial PBS [59] (Copyright in 2015, Nature) and (b) a digital dielectric metamaterial PR [60] (Copyright in 2017, OSA).

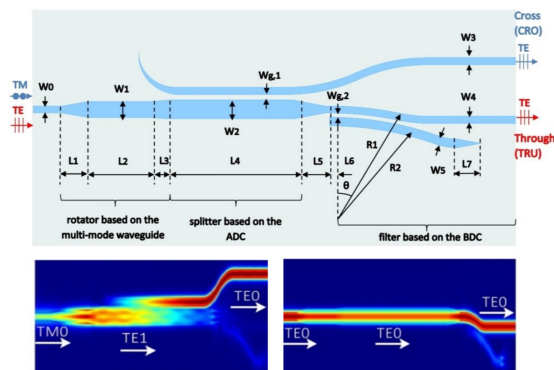


Fig. 16. Layout and simulated field distribution of a PSR based on multimode waveguide [61] (Copyright in 2017, OSA).



Fig. 17. Schematic of a SOI edge coupler based on SWG [64] (Copyright in 2015, OSA).

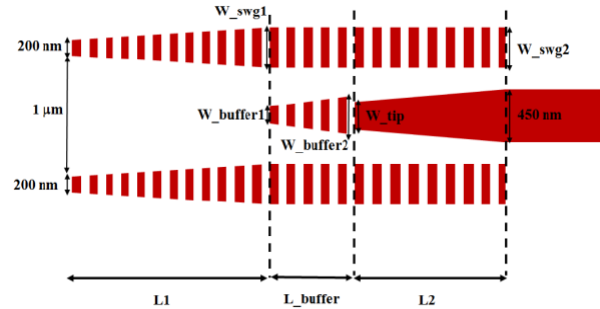


Fig. 18. Schematic of a trident-shape SWG edge coupler [65] (Copyright in 2019, OSA).

in a relatively compact footprint.

C. Compact and Efficient Fiber-to-Chip Coupler

This subsection discusses challenges and recent advances on fiber-to-chip couplers that provide the optical I/Os to IOSP chips. These critical links can limit system performance in terms of insertion loss, bandwidth, power handling, and multimode capabilities. Discussion focuses on the two primary solutions for optical I/Os – edge couplers and grating couplers.

Edge coupling based on spot size conversion is intrinsically broadband and polarization insensitive, however, to couple light from standard SMF28 fiber (large spot size) is still a monumental challenge. Additionally, edge couplers require optical coupling from two edges of the chip, restricting the deployment of waveguide routing. In contrast, grating couplers can handle SMF28 fiber easily but they are narrowband and polarization sensitive. Grating couplers can also be located across the photonic chip, resulting in more flexible mask design and wafer-scale testing [62].

Inverse tapering is the most widely used edge coupling solution to convert the fiber mode into a sub-micron waveguide mode. Lensed fibers or high NA fibers can reduce the mode field diameter (MFD) compared to that of standard SMF28

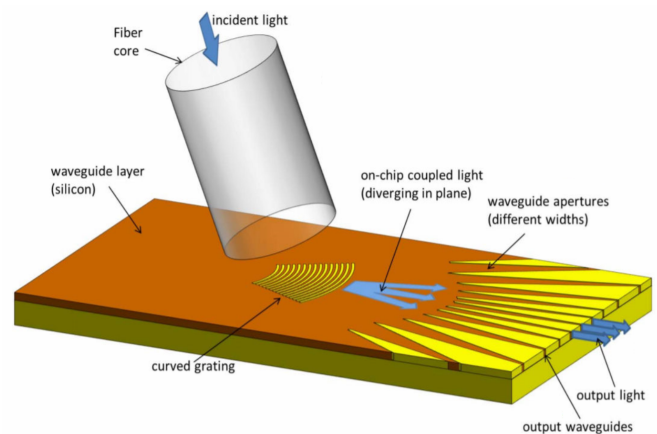


Fig. 19. 3-D illustration of a grating coupler combined with star coupler for high intensity power coupler and splitter [69] (Copyright in 2016, IEEE).

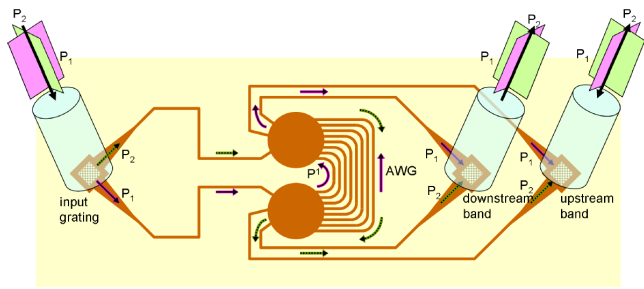


Fig. 20. Schematic of a polarization diverse AWG circuit using 2-D grating coupler [70] (Copyright in 2016, IEEE).

fibers (MFD $\sim 10 \mu\text{m}$) in order to facilitate edge coupling. For example, IBM researchers reported an $875 \mu\text{m}$ long inverse taper based on subwavelength grating (SWG) waveguide that achieved 1.5 dB coupling loss with SMF28 fiber [63]. Less than $100 \mu\text{m}$ long edge coupler would be needed using a similar SWG taper for a lensed fiber ($2.5 \mu\text{m} - 3 \mu\text{m}$ MFD) as shown in Fig.17 [64]. A more compact, trident shape SWG edge coupler was demonstrated, as shown in Fig. 18, while offering relaxed requirements on minimum feature size [65].

Another compelling spot size converter is the inverse taper cladded by a polymer waveguide [66]. Here the cladding creates initial mode confinement, followed by mode transformation into the high-index waveguide core. This design provides a good solution for coupling fibers with large MFD (such as SMF28), since polymer waveguides can be made into arbitrary dimension to match with the input beam profile. The downside comes in the excessive taper length required for efficient mode evolution. To shorten the length, taper shape has been optimized for more efficient mode evolution. One published work [67] shows a taper length reduction from $400 \mu\text{m}$ down to $100 \mu\text{m}$ using a shape-optimized taper instead of a linear taper; this also yielded similar mode conversion efficiency. One study characterized coupling efficiency verse taper length using lensed fibers on the SOI platform; the report showed there exists an optimized taper length where coupling efficiency is maximized [68]. This optimized length provides the best balance of mode transition loss and scattering loss.

Grating couplers, by comparison, are more compact than edge couplers and readily couple the large MFDs from SMF28 fiber. Recent progress has demonstrated integration of grating couplers along with other functionalities, which not only reduce footprint but also provide some additional benefits. For instance, Imec researchers combined a grating coupler and star coupler together to tackle the power handling issue on the SOI platform [69]. Normally high-power signals need to be coupled into one waveguide using standard optical I/O before performing power splitting. However, high power in a single waveguide leads to

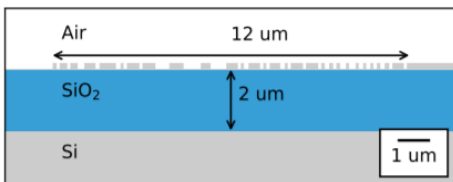


Fig. 21. Schematic of an inverse design grating coupler [71] (Copyright in 2016, IEEE).

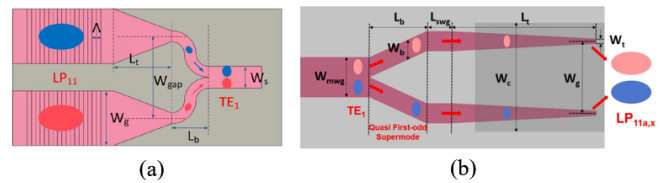


Fig. 22. Schematics of (a) a grating coupler for high order mode coupling [72] (Copyright in 2017, OSA) and (b) an edge coupler for high order mode coupling [73] (Copyright in 2018, OSA).

formidable propagation loss due to two photon absorption. Figure 19 shows a grating coupler integrated with star coupler to directly split the beams from grating diffraction without introducing strong non-linear optical losses [79].

Grating couplers can also be designed to manage polarization diversity [70]. While conventional grating couplers only work for a single polarization, a 2D periodic grating can selectively couple light from two orthogonal fiber polarizations into two coupler outputs; both outputs are coupled into waveguide TE-modes. Consider a polarization diverse AWG circuit, for example. Traditionally this requires two identical AWG devices with polarization handling components. Using 2D grating couplers, however, the polarization handling devices are no longer necessary as shown in Fig. 20. Inverse design was implemented to make the grating coupler device more compact. As shown in Fig. 21, a recent work has reported a grating coupler with a footprint of $12 \mu\text{m} \times 12 \mu\text{m}$ and a -3-dB-coupling bandwidth over 100 nm which is much broader than conventional grating coupler [71].

Another interesting research topic for optical I/O is the coupler that can handle multiple spatial modes. This is one attractive research direction since on-chip MDM systems require interface with optical fibers. Figure 22 demonstrates a grating coupler [72] and edge coupler [73] that can couple between fiber LP_{11} mode and waveguide TE_1 mode. The idea relies on coupling into anti-phase TE_0 pairs and combining into the TE_1 mode.

There are also design efforts to realize spot size converters that concurrently handle fundamental and high order modes [38]. The design is based on the MMI under TE_0/TE_1 excitation where antiphase TE_0 pairs from TE_1 input exit from two outer ports while TE_0 input travels all the way along the middle path. Combined with inverse tapers, both TE_0 and TE_1 inputs from SiN waveguide can couple to the proper modes at polymer waveguide, which works also at TM polarizations. Figure 23 shows the schematic of multimode spot size converter that

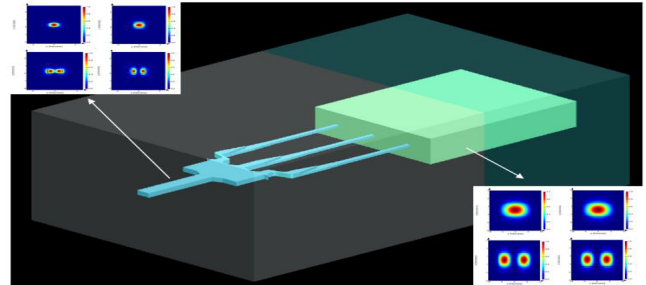


Fig. 23. 3-D illustration of a SiN spot size converter that can sumptuously couple TE_0 , TE_1 , TM_0 and TM_1 modes to a low-index-contrast polymer waveguide [38].

supports four spatial modes (TE_0 , TE_1 , TM_0 and TM_1).

III. DISCUSSION AND CONCLUSION

Ultra-fast switching functionalities are an important category of capability for IOSPs complementary to the new building blocks of passive silicon devices. As a basic building block, the Mach-Zehnder modulator (MZM) is a critical component for the construction of compact MIMO ultra-fast switch arrays on the silicon photonics platform. It provides high bandwidth, low $V\pi$ /switching voltage, high power extinction, and miniaturized size suitable for integration with other processor building blocks. Lithium niobate (LN) electrooptic (EO) modulators stand out among all of the materials explored for MZMs [74–79] that target switching speeds < 20 ps (bandwidth > 50 GHz) for application to ultra-fast signal processing and computing. Their superior optical properties include modulation bandwidth of up to 100 GHz, low propagation loss < 1 dB/cm, low $V\pi \cdot L < 3$ V·cm, high power extinction > 20 dB, chirp-free operation, device robustness, and wide wavelength transparency from 0.4 μm to 5 μm [75]. Traditional LN waveguides fabricated by indiffusion of Ti atoms or proton-exchange methods [78] are bulky and require a length of several centimeters to provide a $V\pi$ around 3 V; these are not suitable for highly integrated optical processors.

A novel thin film technology has recently been explored which supports much more compact LN devices on silicon substrates, i.e., LNOI devices. As reviewed elsewhere [75, 79], waveguide core size and bending radius of LN devices can be reduced by one to two orders of magnitude. This approach has great potential for integrating LNOI modulators/switches into IOSP chips as illustrated in Fig. 2; the waveguide mesh network and other passive functionalities discussed above have already been demonstrated in SOI waveguides. However, further investigations are needed to verify practicality and scalability of LNOI-based components in IOSP chips.

The heterogeneous integration methods that have enabled LNOI devices may also be used to integrate semiconductor optical amplifiers (SOAs) in IOSPs; integration of such active components could enable on-chip laser sources along with new signal processing capabilities to widely increase the range of IOSP applications. For example, few-mode SOAs can perform four-wave mixing with high conversion efficiency over a broad detuning bandwidth [80, 81] to support optical mode manipulation. Recently, a few-mode SOA demonstrated inter-modal degenerate four-wave mixing with a 10-dB improvement in efficiency compared to a single-mode counterpart over a frequency detuning of ± 400 GHz [81]. While such devices point to on-chip nonlinear signal processing functionalities such as all-optical switches and wavelength converters, the performance issues on noise and crosstalk as well as requirements for device temperature control remain practical concerns for their use in IOSPs.

Regarding the waveguide mesh network, other network architectures with further reduction of the mesh cell size are possible with the TBUs implemented using optical micro-ring resonators (MRRs) instead of MZIs. MRR-based mesh networks have been previously studied for $N \times N$ optical switch

networks, and similar architectures can also be considered for integrated optical signal processor chips. MRRs can be made in very compact forms, with a very small waveguide bend radius, e.g., < 5 μm , when implemented in SOI waveguides. Like MZIs, thermo-optical or electrooptical tuning mechanisms can provide on-off switching from MRRs to control routing across a mesh network of waveguides. For example, silicon MRR modulators (switches) in carrier-depletion type can provide a modulation bandwidth > 30 GHz [82–84]. While small footprint and low power consumption are promising features of these devices, thermal and fabrication tolerance as well as their limitation on operation wavelength range remain as challenges for practical use [85].

Continued advancements in photonic integration technology is crucial to drive the development of IOSPs to empower future communications, networking and computing applications. As new building blocks for the hardware platform, several miniaturized passive silicon devices and potential switching devices are discussed to support extension of processor capabilities and enable ultra-dense integration of complex PICs. The results shown in this paper reflect the significance and maturity of the state-of-the-art photonics fabrication technology and contribute to the implementation of high-capacity, general-purpose optical signal processing functionalities on the chip scale.

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