MITSUBISHI ELECTRIC RESEARCH LABORATORIES
http://www.merl.com

Gate Leakage Mechanisms and Modeling in GaN based High Electron Mobility Transistors – Literature Survey

Li, Kexin; Teo, Koon Hoo

TR2019-160 December 20, 2019

Abstract

This is a survey report on the reliability issues of Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT). It particularly focused on the reliability issue of the device gate leakage.

Mitsubishi Electric Research Laboratories

MITSUBISHI ELECTRIC
Changes for the Better

for a greener tomorrow

Gate Leakage Mechanisms and Modeling in GaN based High Electron Mobility Transistors – Literature Survey

Kexin Li and Koon Hoo Teo

June 10, 2019

Contents

Gallium nitride based HEMTs

Gallium nitride (GaN)-based transistors have experimentally demonstrated potential for implementing both high voltage switching devices, and high-power RF amplifiers. III-nitride HEMTs are also more attractive than GaAs and InP technologies for building RF power amplifiers because of their improved maximum output power, potentially up to 300 GHz [1]. Further, the high current capability of III-nitride heterostructures relative to silicon carbide devices provides an advantage to III-nitride technology for high frequency operation and higher RF output power above X band frequencies [2,3].

Even in the absence of external doping, GaN-based heterostructures provide high polarization-induced carrier concentration and high carrier velocities (Fig.1). Taking $Al_xGa_{1-x}N/GaN$ heterojunction as an example, the spontaneous[1] and piezoelectric[2] polarizations result in a 2DEG with a high carrier concentration on the GaN side of the heterojunction (6×10^{12} to 2×10^{13} cm^{-2} as Al composition x increases from 0.15 to 0.31) [4]. However, the lattice mismatch resulting in a large value of the piezoelectric polarization in AlGaN/GaN heterostructures also makes the fabrication of high-quality and stress-free GaN-based epilayers challenging. Alternative materials and novel device structures, such as lattice-matched InAlN/GaN, have been proposed to optimize the HEMT performance [5].

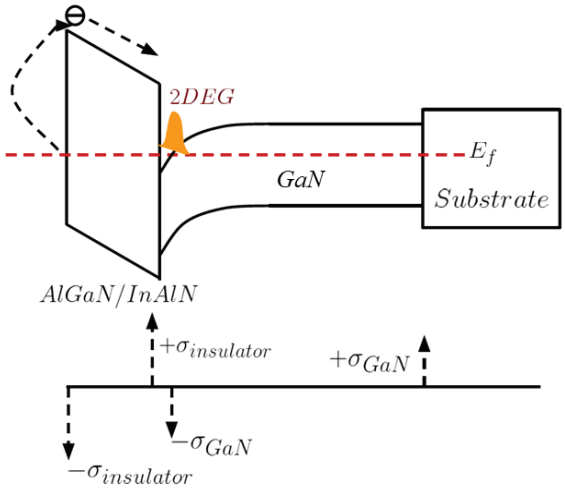

Figure 1Polarization-induced charge in AlGaN- and AlInN-based HEMTs with GaN channel (Figure Source Ref.[6]).

[1] Spontaneous polarization (SP) is caused by an intrinsic asymmetry of the bonding in the equilibrium Wurtzite crystal structure.
[2] Piezoelectric polarization (PZ) is due to mechanical stress. Negative for tensile and positive for compressive strained insulator (e.g. AlGaN) layers.

Reliability: Gate leakage

The development of GaN high electron mobility transistors (HEMTs) technology in high frequency and high power applications is bottlenecked by its limited electrical reliability. Gate leakage is one of the major problems plaguing these devices. Because HEMT devices on III-nitride materials are normally on devices with high 2DEG concentration, large negative bias is necessary to turn off the device. Thus the gate leakage becomes significant in dividing the standby power dissipation and the reliability of the device.

Mechanisms and modeling of Gate leakage

The dominate mechanisms causing gate leakage current varies based on biasing and temperature conditions. As shown in Fig. 2, while the forward leakage current is dominated by thermionic emission (TE), the observed reverse leakage current in GaN based HEMTs are much larger than the predicted by thermionic emission [7]. Poole-Frenkel emission (PFE) and Trap-assisted tunneling (TAT) have been said to be the dominant leakage mechanisms for gate current conduction at higher temperature under medium and low reverse bias; Fowler-Nordheim tunneling (FNT), which is independent of temperature, is also observed under large reverse bias [7-13]. And it is observable since PFE no longer dominate at low temperature. Details of each will be discussed separately as follow.

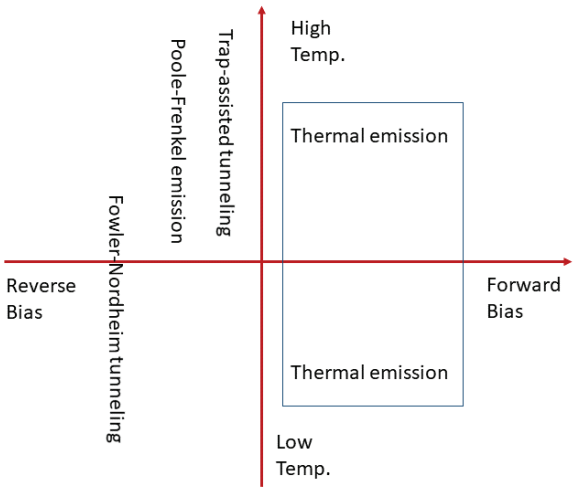

Figure 2Mechanisms causing gate leakage under different bias and temperature conditions.

The contribution of each gate leakage mechanisms could be different based on the heterostructure also. As shown in Fig. 3, gate leakage current versus gate voltage for both AlGaN/GaN and AlInN/GaN HEMTs are measured and modeled in Ref. [7], with leakage current due to each mechanism shown for reference.

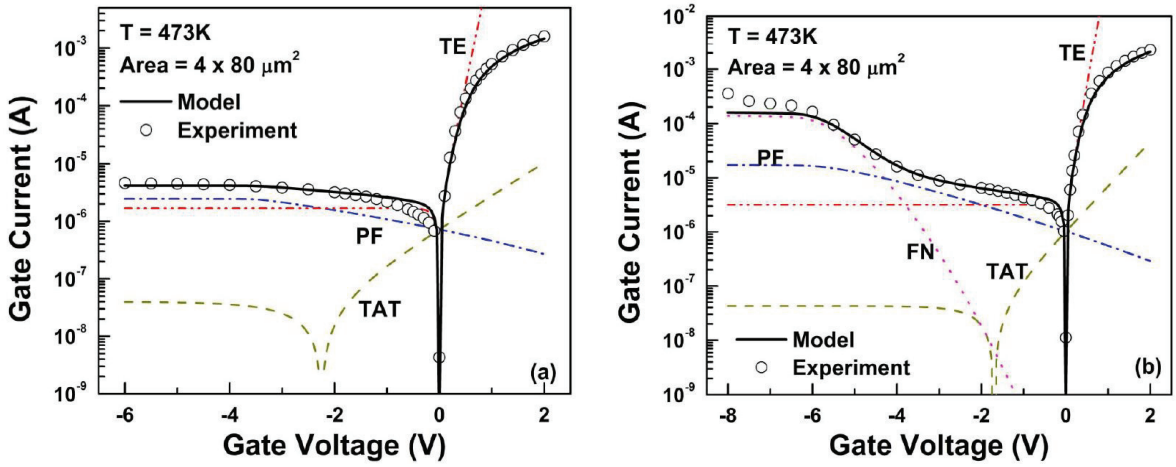

Figure 3 Gate leakage current versus gate voltage of AlGaN/GaN (left) and AlInN/GaN (right) HEMT. Various components are shown for reference. Model fit and figure source: Ref.[7].

Thermal emission (TE):

Under forward bias, gate current due to thermal emission is the dominate one. The relation between current density and voltage drop across Schottky barrier J_{TE}-V is described by expression [7]:

$$J_{TE} = J_0\left\{exp\left(\frac{q(V)}{\eta kT}\right) - 1\right\} \Rightarrow ln\, J_{TE} \approx ln\, J_0 + \frac{qV}{\eta kT} \qquad (1)$$

$$J_0 = AT^2\, exp\left(-\frac{q\phi_b}{kT}\right) \rightarrow ln\, J_0 = ln\, A + 2\, ln\, T - \frac{q\phi_b}{kT} \qquad (2)$$

With all the related parameters are listed in Tab. 1.

J_0	Reverse saturation current density
A	Effective Richardson's constant
T	Absolute temperature
q	Electron charge (1.6×10^{-19})
ϕ_b	Schottky barrier height
η	Ideality factor
k	Boltzmann's constant ($1.38 \times 10^{-23}\ J/K$)

Table 1 Parameters related to the TE current.

The parameter $J_0(\phi_b)$, η, can be extracted based on the intercept and slope of the $\ln J_{TE}$ versus V ($V > 3kT$) as shown in Fig. 4 (left).

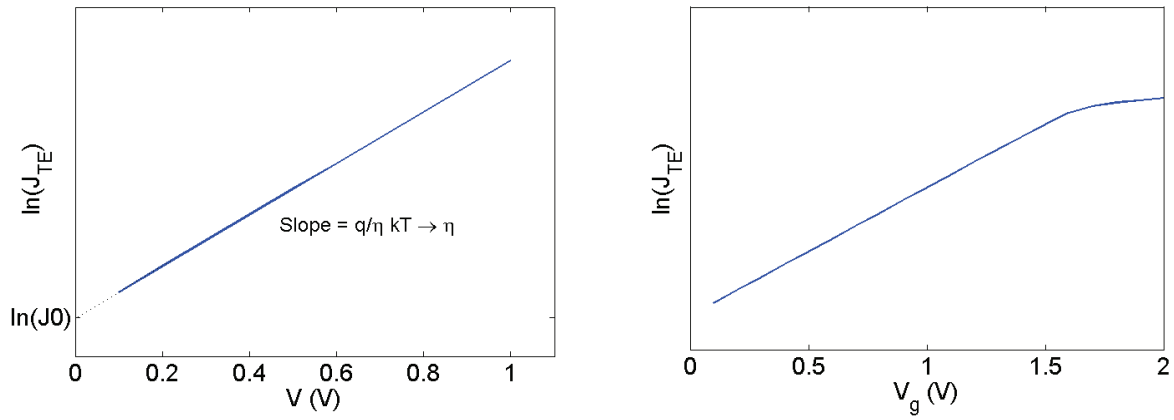

Figure 4 Typical plot of ln(J_{TE}) versus voltage V applied on the Schottky barrier only (left) and ln(J_{TE}) versus gate bias Vg applied on GaN based HEMTs (right).

The slope of $\ln J_{TE}$ versus V is proportional to T^{-1}. While the reverse saturation current J_0 will increase with temperature. The Schottky barrier height can be extracted based on

$$\phi_b = \frac{kT}{q}[ln\, A + 2\, ln\, T - ln\, J_0] \quad (3)$$

In case of a GaN based HEMTs, the expression of the TE current with respect to gate bias should be modified as

$$J_{TE} = J_0\left\{exp\left(\frac{q(V_g-\psi)}{\eta kT}\right) - 1\right\} \quad (4)$$

, where ψ is the channel potential which will varies along the current flow direction. As shown in Fig. 3, in the forward bias region, following Eq. 1, the current has to increase exponentially with applied voltage. However, the gate leakage current as measured in semi-logarithmic I-V characteristics plot deviate from the straight line at large forward bias. Fig. 4 (right) shows a qualitative plot of current density with respect to gate bias applied on GaN based HEMTs, by modeling it as adding a series resistance to the Schottky barrier in which thermal emission current dominates.

Poole-Frenkel emission (PFE):

Under low to medium reverse bias, the reverse leakage current is dominated by Poole-frenkel emission current and Trap-assisted tunneling. PFE is the electric field-enhanced thermal emission of electrons from a trap state to the continuum states associated with a conductive dislocation [7-13]. In order to describe this mechanism, conduction band under medium applied gate bias is shown below. The PFE has a strong temperature dependence.

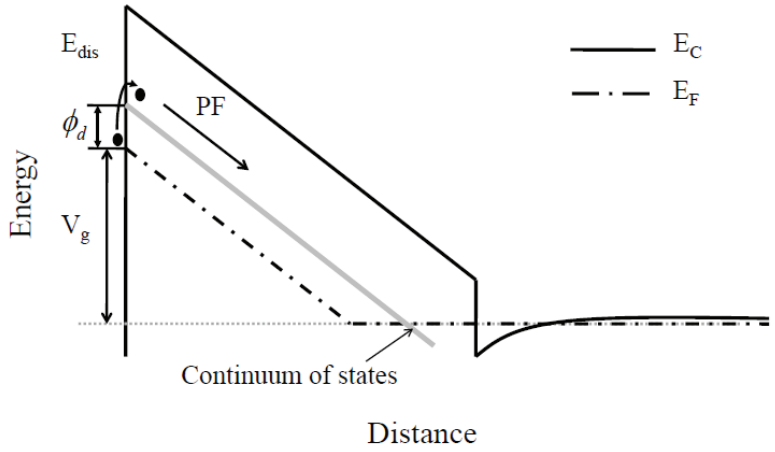

Figure 5 Conduction band diagram of AlGaN/GaN HEMT for medium reverse gate voltage showing the electric field-enhanced thermal emission of electrons from a trap state to the continuum states associated with a conductive dislocation (Ref. [8]).

The current density J_{PF} as function of electric field (E) is expressed as

$$J_{PF} = CE\, exp\left[-\frac{q(\phi_d - \sqrt{(qE/\pi\varepsilon_i)})}{kT}\right] \quad (5)$$

C	Constant depends on trap concentration
ϕ_d	Barrier height for electron emission from the trap state
ε_i	Permittivity of the semiconductor at high frequency

Table 2 Parameters related to the PFE current

$$ln\left(\frac{J_{PF}}{E}\right) = ln(C) - \frac{q\phi_d}{kT} + \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_i}}\sqrt{E} = c(T) + m(T)\sqrt{E} \quad (6)$$

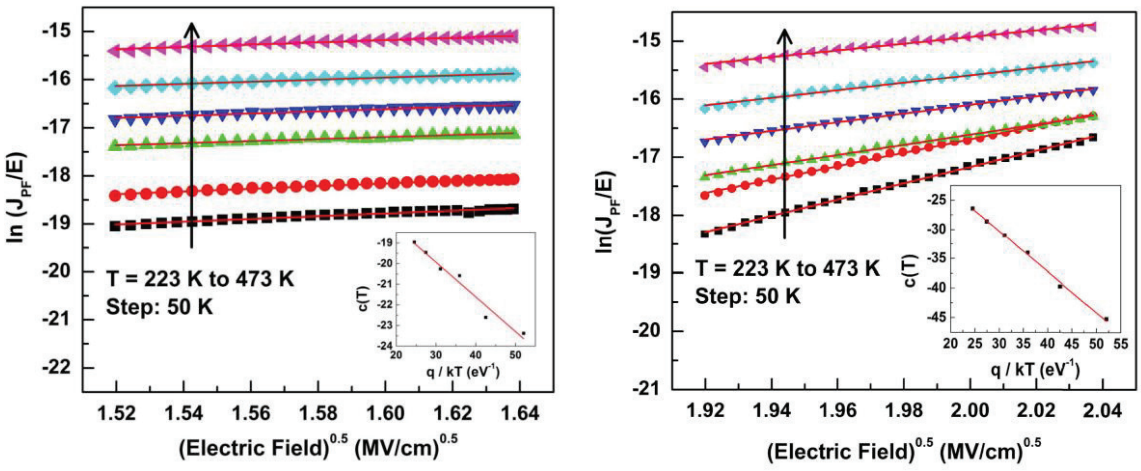

Figure 6 Typical plot of ln(J_{PF}/E) versus $\sqrt{E}$ measured under various temperature. Subfigure shows the extracted value of c(T) versus temperature based on the intercept. (left) AlGaN/GaN, (right) InAlN/GaN. Figure source: Ref. [7]

By converting Eq.5 into the form shown in Eq.6, the plot of $\ln(J_{PF})/E$ versus $\sqrt{E}$ yields straight lines under different temperature as expected. And the intercept and slope can be used to extract c(T), and m(T).

The electric field across the barrier is calculated using the expression

$$E = \frac{q(\sigma_p - n_s)}{\varepsilon_i} \quad (7)$$

σ_p	Bound charge at the hetero-interface, sum of PZ and SP polarization
n_s	2DEG concentration at the hetero-interface

Table 3 Parameters related to calculate electric field across the barrier.

, where the 2DEG charge concentration n_s is a function of gate bias and channel potential ψ. Thinner barrier and higher electric field across the barrier results in carrier tunneling through the barrier, leading to large gate leakage current.

The difference between the TAT and PFE is the source of the source of electrons. For TAT, electrons tunnel from metal to semiconductor through a band of localized traps present in AlGaN layer. While for the PFE, the electron comes from trap state.

Trap-assisted tunneling (TAT):

Around zero gate bias, electrons tunnel from metal to semiconductor through a band of localized traps present in insulator (AlGaN/InAlN) layer. This defect-assisted tunneling current flows from gate to the channel to compensate for the Poole-Frenkel emission current flowing from the channel to the gate near zero bias [7-9]. It has the same temperature dependence as that of PF emission current.

$$J_{TAT} = J_{02}\left\{exp\left(\frac{q(V_g - V_0 - \psi)}{\eta_2 kT}\right) - 1\right\} \quad (8)$$

J_{02}	Reverse saturation current density
V_0	Voltage used to fit the experimental data close to origin
η_2	Ideality factor

Table 4 Parameters related to the TAT current.

Same as thermal emission, ψ is the channel potential. The reverse saturation current density can be calculated by equaling J_{TAT} to J_{PF} at zero gate bias. And $\ln(J_{TAT})$ versus $V_g - V_0 - \psi$ shall yield straight line with slope $\frac{q}{\eta_2 kT}$ and intercept $\ln(J_{TAT})$.

Fowler-Nordheim tunneling (FNT):

Under high reverse gate bias, the electric field across the insulator (AlGaN/InAlN) barrier layer is too high, and it reduces the thickness of the barrier at the metal fermi level. As shown in Fig. 6, Electrons from gate metal can easily tunnel across this thin triangular barrier, adding Fowler-Nordheim tunneling(FNT) [7-10]. The FNT current also depends on

the allow composition in the material, For example, AlGaN/GaN device with higher Al composition introduce more electric field across the barrier resulting in more FNT current. The FNT current is independent of temperature. It becomes the dominate component when PFE current becomes low at lower temperature. The higher the Al mole fraction in AlGaN/GaN devices, the higher temperature FNT current becomes dominate.

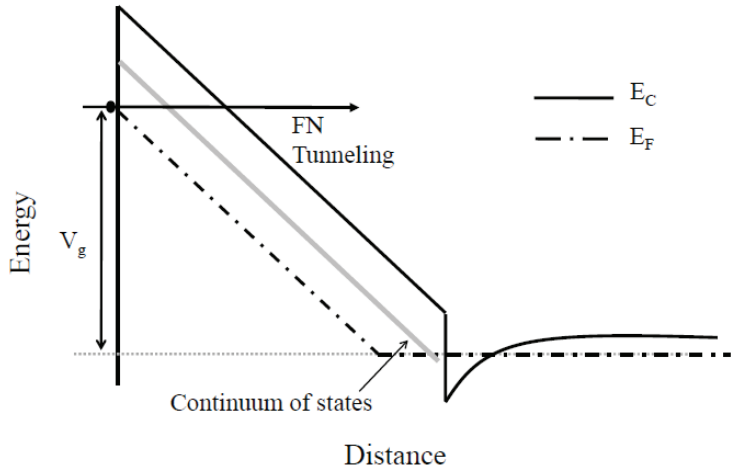

Figure 7 Conduction band diagram of AlGaN/GaN HEMT in high reverse gate voltage shows the FN tunneling mechanism (Ref. [8]). High electric field reduces the rhickness of the barrier at the metal Fermi level, and from gate metal electron can easily tunnel across.

The $J_{FN} - E$ expression according to Ref.[7] is

$$J_{FN} = AE^2 \, exp\left(-\frac{B}{E}\right) \quad (9)$$

$$B = \frac{8\pi\sqrt{2m_n^*(q\phi_{eff})^3}}{3qh} \quad (10)$$

A	Constant
m_n^*	Conduction band effective mass in semiconductor
h	Planck's constant
ϕ_{eff}	Effective barrier height

Table 5 Parameters related to the FNT current

, where the electric field at the metal-AlGaN layer is calculated same as PFE.

$$ln\left(\frac{J_{FN}}{E^2}\right) = ln(A) - \frac{B}{E} \quad (11)$$

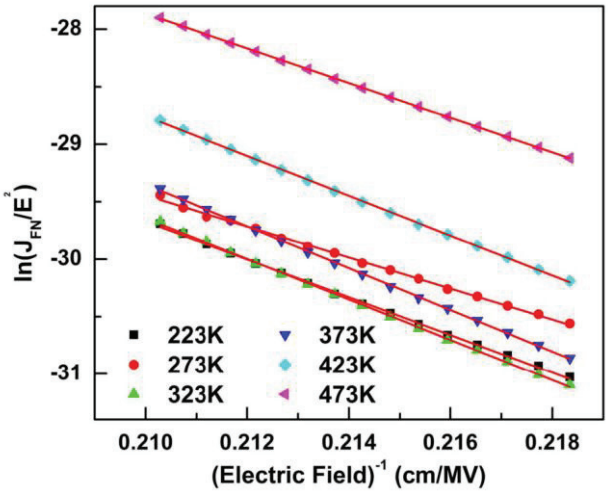

Figure 8 Typical plot of ln(J_{FN}/E^2) versus E^{-1} measured under various temperature. Figure source: Ref. [7]

The straight lines given by plotting $\frac{\ln J_{FN}}{E^2}$ versus E^{-1} indicate the value of $\ln(A)$, and B.

My suggestion on Gate Leakage current modeling

Gate leakage cureent modeling based on channel potential profile:

According to the expressions of J_{TE}, J_{TAT}, J_{PF}, and J_{FN}, the dependency on channel potential ψ suggests the total current has to be achieved by integrate the current density along the channel length from the source to the drain.

$$I_{tot} = W \int_0^L J_{TE} + J_{TAT} + J_{PF} + J_{FN}\, dx \qquad (12)$$

And the integration variable has to be convert from x to ψ.

In case of long channel potential ψ, according to Ref. [8], similar approach has been taken out for long channel devices where gradual channel approximation is available through the channel. The conversion from x to ψ is based on:

$$dx = \frac{L(V_g - V_{off} - \psi + kT/q)}{(V_{g0} - \psi_m + kT/q)(\psi_d - \psi_s)} d\psi \qquad (13)$$

However, for short channel device, the GCA is only valid at the top of the barrier (ToB), noted as x_0, in the channel. This means that Eq. 13 is not valid any more.

The channel potential profile obtained by solving the 2D Poisson equation has been estimated for short channel GaN based devices as explained in Ref.[14]. The channel potential with repect to the potential at the ToB under off- and on- states as generated by TCAD numerical simulation tool Sentaurus (Fig. 9) can be modeled based on

$$\psi(x) - \psi(x_0) \approx \eta_s \frac{sinh\left(\frac{L-x}{\lambda_{sl}}\right)}{sinh\left(\frac{L}{\lambda_{sl}}\right)} + \eta_d \frac{sinh\left(\frac{x}{\lambda_{sl}}\right)}{sinh\left(\frac{L}{\lambda_{sl}}\right)} \quad (14)$$

, where λ_{sl} depends on the channel properties and is referred to as the scaling length. It signifies the rate of change of channel potential from source/drain to the channel center. While η_s refers to the potential change at the ToB due to applide bias, and $\eta_d - \eta_s = V_{dsi}$.

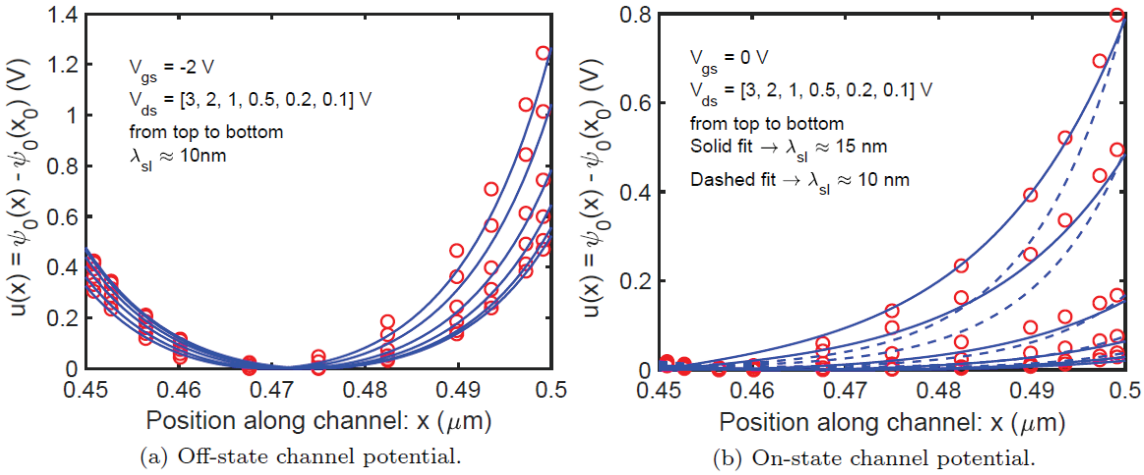

Figure 9 Channel potential profile in (a) off- and (b) on-state of 50 nm gate length AlGaN/GaN HEMT. Symbols represent numerical simulation results, solid lines correspond to model fit using Eq. 14. Figure source: Ref.[14].

While Eq. 14 is strictly valid in off-state, it is used to explain the channel profile in both off- and on-states by adjusting value of λ_{sl}.

The model of total gate leakage current could be re-derived based on this updated channel potential profile.

Advanced device structure with optimized gate leakage current:

AlGaN/GaN based metal-oxide-semiconductor heterostructre field-effect transistor (MOSHFET) has been reported for reducing the gate leakage current [15,16].

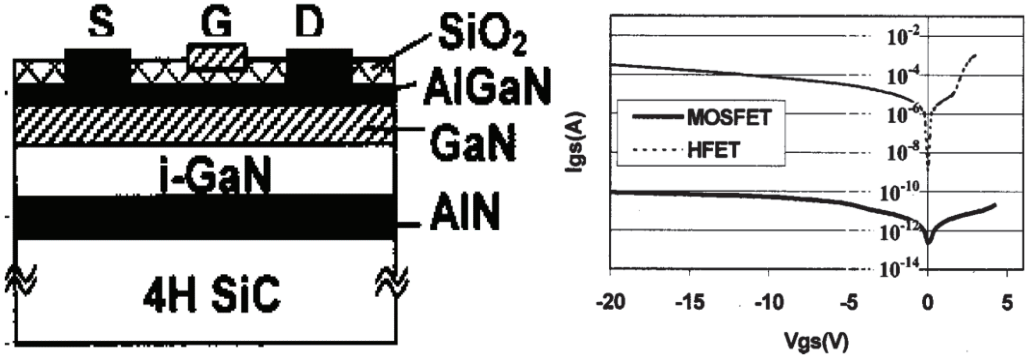

Figure 10 Heterostructure of AlGaN/GaN MOSHFET, and its gate leakage current compared with baseline HFET. Figure source (Ref.[16]).

The gate leakage current model of this optimized device structure has not been discussed so far.

References

[1] Chung, Jinwook W., et al. "AlGaN/GaN HEMT With 300-GHz f_{max}." *IEEE Electron Device Letters* 31.3 (2010): 195-197.

[2] Sheppard, S. T., et al. "High-power microwave GaN/AlGaN HEMTs on semi-insulating silicon carbide substrates." *IEEE Electron Device Letters* 20.4 (1999): 161-163.

[3] Wu, Y-F., et al. "30-W/mm GaN HEMTs by field plate optimization." *IEEE Electron Device Letters* 25.3 (2004): 117-119.

[4] Ambacher, O., et al. "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N-and Ga-face AlGaN/GaN heterostructures." *Journal of applied physics* 85.6 (1999): 3222-3233.

[5] GONSCHREK, M. "High Electron Mobility Lattice-matched AlInN/GaN Field-Effect Transistor Heterostructures." *Appl. Phys. Lett.* 89 (2006): 062102.

[6] Li, Kexin, and Shaloo Rakheja. "Optimal III-nitride HEMTs: from materials and device design to compact model of the 2DEG charge density." *Gallium Nitride Materials and Devices XII*. Vol. 10104. International Society for Optics and Photonics, 2017.

[7] Turuvekere, Sreenidhi, et al. "Gate leakage mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: comparison and modeling." *IEEE Transactions on electron devices* 60.10 (2013): 3157-3165.

[8] Ghosh, Sudip, et al. "Physics based Modeling of Gate Current including Fowler-Nordheim Tunneling in GaN HEMT."

[9] Mojaver, Hassan Rahbardar, and Pouya Valizadeh. "Reverse gate-current of AlGaN/GaN HFETs: Evidence of leakage at mesa sidewalls." *IEEE Transactions on Electron Devices* 63.4 (2016): 1444-1449.

[10] Zhang, H., E. J. Miller, and E. T. Yu. "Analysis of leakage current mechanisms in Schottky contacts to GaN and Al 0.25 Ga 0.75 N⁄ Ga N grown by molecular-beam epitaxy." *Journal of Applied Physics* 99.2 (2006): 023703.

[11] Yan, Dawei, et al. "On the reverse gate leakage current of AlGaN/GaN high electron mobility transistors." *Applied Physics Letters* 97.15 (2010): 153503.

[12] Chikhaoui, W., et al. "Current deep level transient spectroscopy analysis of AlInN/GaN high electron mobility transistors: Mechanism of gate leakage." *Applied Physics Letters* 96.7 (2010): 072107.

[13] Arslan, Engin, Serkan Bütün, and Ekmel Ozbay. "Leakage current by Frenkel–Poole emission in Ni/Au Schottky contacts on Al 0.83 In 0.17 N/AlN/GaN heterostructures." *Applied Physics Letters* 94.14 (2009): 142106.

[14] Li, Kexin, and Shaloo Rakheja. "A unified static-dynamic analytic model for ultra-scaled III-nitride high electron mobility transistors." *Journal of Applied Physics* 125.13 (2019): 134503.

[15] Stoklas, R., et al. "Gate leakage reduction of AlGaN/GaN MOS-HFETs with HfO 2 prepared by ALD." The Tenth International Conference on Advanced Semiconductor Devices and Microsystems. IEEE, 2014.
[16] Khan, M. Asif, et al. "AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect transistors on SiC substrates." Applied Physics Letters 77.9 (2000): 1339-1341.