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Abstract

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***Abstract*—This paper proposes a new system architecture to reduce the hardware cost for a digital beamforming (DBF) transmitter array. In a conventional DBF transmitter array, each signal channel requires a digital-to-analog converter (DAC) to convert the digital signal to the analog signal, so that the cost and power consumption for such systems are often prohibitively high as the array size increases. In the proposed DBF transmitter array system, code-division multiplexing (CDM) technique is used to combine digital signals from different channels, and thus the required number of DACs can be significantly reduced. The combined signal is separated by demodulation with the corresponding code sequences for each channel after the DAC. Principle of CDM for hardware reduction in a DBF array system is analyzed. A system-level simulation is performed in Simulink to verify the performance of the proposed system. Simulation results show that the beamforming accuracy and signal quality can be maintained with a reduced number of DACs.**

***Index Terms*—Digital beamforming, code-division multiplexing, phased array.**

I. Introduction

Beamforming technology is critical for a phased array system. Conventional phase shifter based RF beamforming systems suffer from issues such as phase errors, resolution, and bandwidth [1], [2]. For large arrays, which has been adopted in the next generation cellular communication system, these issues will become even worse. By moving the beamforming part to the digital domain, which is referred to as the digital beamforming (DBF) system, the resolution limitation of the conventional phase shifter based RF beamforming systems can be overcame [3], [4]. However, a DBF system requires the duplication of major components for each signal channel, which makes the hardware extremely complicated. Moreover, high-speed analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) are required for a broadband and large array DBF system. These high speed analog-digital mixed devices are known to have high cost and high power consumption [5]. Innovations to simplify the hardware and reduce the required number of analog-digital mixed devices in a DBF system is highly appealing.

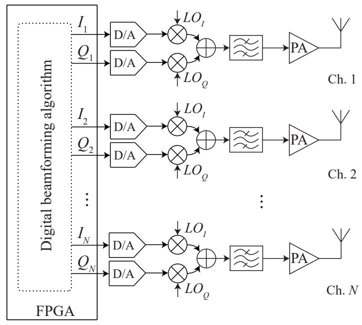

Fig. 1. Top-level block diagram of a conventional DBF transmitter array.

One approach to reduce the hardware of a DBF system is to adopt multiple-access techniques to share the hardware. Time-division multiplexing (TDM), code-division multiplexing (CDM), and frequency-division multiplexing (FDM) are three widely used multiple-access techniques in wireless communications to share a single wireless channel for different terminals. For example, the "spatial multiplexing of local elements array (SMILE)" system utilized TDM to share the RF paths [6]. CDM has also been proposed in wideband and multi-band DBF receivers to reduce the number of ADCs [7], [8], [9]. The performance of different code sets has also been analyzed in Ref.[7]. However, all previous work based on multiple-access techniques focus only on the receiver system, in which de-muxing or the de-coding process can be realized relatively easy in digital domain. For a DBF transmitter array system, the de-muxing or the de-coding process has to be realized in analog domain. The idea of utilizing CDM in a DBF transmitter array system was not presented so far to the best of our knowledge.

In this paper, a method to reduce the hardware for a DBF transmitter array system is proposed. In the digital domain, signals from different channels are modulated with orthogonal codes and then combined

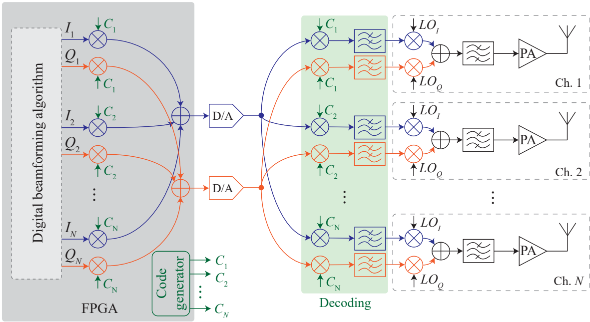

Fig. 2. Proposed CDM-based DBF transmitter array for hardware reduction.

together. The combined signal goes through one single DAC. After the DAC, signals of different channels are separated through a de-modulation process. The design principle of the proposed code-modulation for hardware reduction in a DBF transmitter array system is presented. A system-level simulation was performed in Simulink to verify the performance of the proposed system with a reduced number of DACs, including beamforming accuracy and signal quality.

This paper is organized as follows. Section II addresses the design principle of the proposed CDM-based hardware-reduced DBF transmitter array system. In Section III, system-level simulation with Simulink is performed and analyzed. Section IV draws the conclusion.

II. Design Principles

Figure 1 is the top-level block diagram of a conventional DBF transmitter array system. It can be seen that each channel requires a replica of two DACs, a frequency up-converter, a band-pass filter and a power amplifier (PA). The DACs are usually high cost and high power consumption. For a large transmitter array, the cost and power consumption are almost proportional to the number of DACs. Thus, it is very important to find a method to reduce the number of DACs in order to lower the cost and power consumption.

The block diagram of the proposed CDM-based hardware-reduced DBF transmitter array is illustrated in Fig. 2. The proposed transmitter array has a digital processor, which can be an FPGA. N-channel weighted quadrature digital baseband signals are modulated with orthogonal code sequences. The modulated signals are combined into I/Q signals. Two DACs are used to convert the digital I/Q signals into the analog I/Q signals. In analog domain, different channel signals are separated by de-modulation process and low-pass filtering. The de-modulation process is done by mixing the combined signal with the corresponding orthogonal code sequence generated by the FPGA directly. After separation, signal in each channel is up-converted, filtered, amplified and transmitted.

The modulated and combined digital can be written as:

$$\begin{aligned} y[n] &= x[n]\boldsymbol{w} \times \boldsymbol{C[n]} \\ &= \sum_{i=1}^{N} x[n] w_i C_i[n] \end{aligned} \tag{1}$$

where $x[n]$ is the modulated baseband signal. $\boldsymbol{w} = [w_1, w_2, ..., w_N]$ is the beamforming weight array. n is sample numbers. N is the size of the array. $\boldsymbol{C[n]}$ is the array of N orthogonal code sequences, and

$$\boldsymbol{C[n]} = [C_1[n], C_2[n], ..., C_N[n]]^T \tag{2}$$

where T is the transpose of the array.

Digital signal $y[n]$ is converted into analog signal $y(t)$ through the DACs:

$$y(t) = \sum_{i=1}^{N} x(t) w_i C_i(t) + e \tag{3}$$

where $C_i(t)$ is the analog sequence of i-th orthogonal sequence and $x(t)$ is the analog baseband signal. e is quantization noise.

In order to separate the combined signal, $y(t)$ is mixed with the corresponding code sequence:

$$s_k(t) = \sum_{i=1}^{N} x(t) w_i C_i(t) C_k(t) + C_k(t) e \tag{4}$$

where $s_k(t)$ is the separated signal on k-th channel. Since the code has values either 1 or -1, the statistics of quantization noise term $C_k(t)e$ after the mixing does not change.

It has been discovered that the orthogonal codes are necessary to faithfully recover the signal on each channel. In this paper, Walsh codes are used. Table I lists the eight-bit Walsh codes. From Table I, it is easy to find:

$$C_i(t)C_k(t) = \begin{cases} 1 & \text{if } i = k \\ 0 & \text{if } i \neq k \end{cases} \tag{5}$$

For $i \neq k$, the minimal frequency of the square sequences of $C_i(t)C_k(t)$ is $1/(8T_c)$, where T_c is code period and $1/T_c$ is code rate. Thus, if the bandwidth (BW) of the baseband signal $x(t)$ is smaller than $1/(16T_c)$, the contribution terms $x(t)w_iC_i(t)C_k(t)$ $(i \neq k)$ can be filtered through a low-pass filter. Finally, the signal of each channel can be fully recovered:

$$s'_k(t) = x(t) w_k + C_k(t) e \tag{6}$$

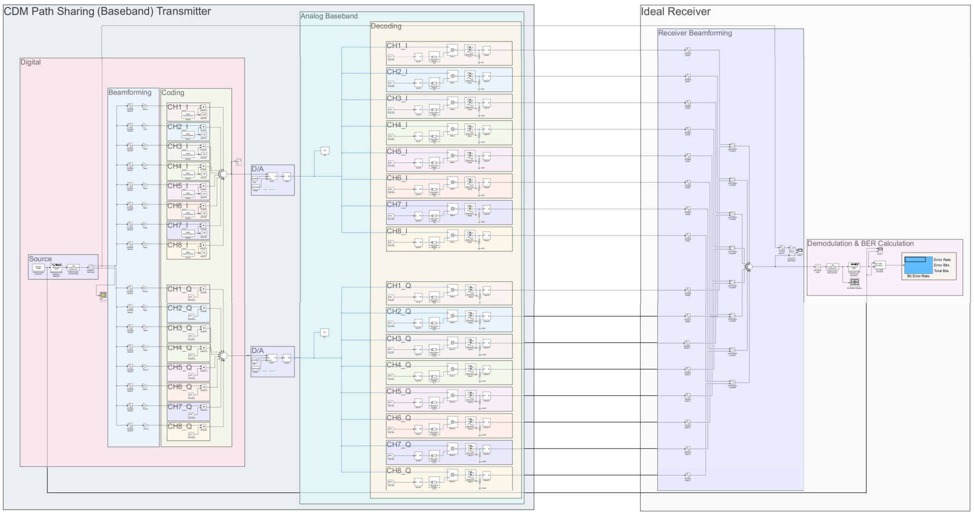

Fig. 3. Simulink model of the proposed DBF transmitter array system.

TABLE I
EIGHT-BIT WALSH CODES.

Index								
0	1	1	1	1	1	1	1	1
1	1	1	1	1	-1	-1	-1	-1
2	1	1	-1	-1	-1	-1	1	1
3	1	1	-1	-1	1	1	-1	-1
4	1	-1	-1	1	1	-1	-1	1
5	1	-1	-1	1	-1	1	1	-1
6	1	-1	1	-1	-1	1	-1	1
7	1	-1	1	-1	1	-1	1	-1

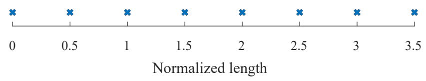

Fig. 4. Antenna array configuration.

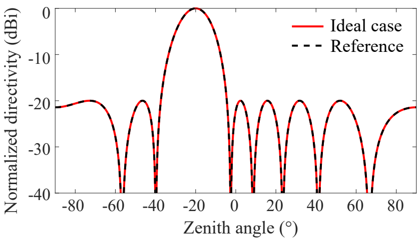

Fig. 5. Beam pattern of the ideal case for the proposed system.

TABLE II
BEAMFORMING WEIGHT VALUES.

Element	Weight	Element	Weight
1	$0.58 + 0.00j$	**5**	$-0.40 + 0.91j$
2	$0.31 - 0.58j$	**6**	$0.53 + 0.69j$
3	$-0.48 - 0.73j$	**7**	$0.65 - 0.11j$
4	$-1.00 + 0.08j$	**8**	$0.19 - 0.55j$

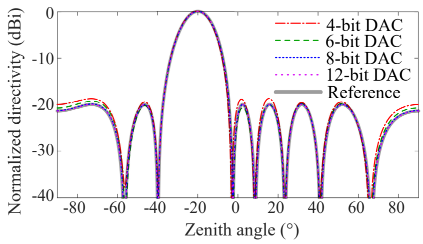

Fig. 6. Beam patterns for the system with different DAC resolutions.

TABLE III
SIDE LOBE ERRORS WITH DIFFERENT DAC RESOLUTIONS.

DAC resolution (bits)	4	6	8	12
Side lobe error (dB)	4.16	1.18	0.19	0.01

III. SIMULATION RESULTS

A system-level model of the proposed CDM-based DBF transmitter array is created with Simulink. Fig. 3 shows the Simulink model of the proposed transmitter, as well as an ideal receiver. In the Simulink model, signals from eight channels ($N = 8$) are combined to share one DAC. Eight-bit Walsh codes are used for modulation and de-modulation. The bandwidth of $x(t)$ is 12 MHz. Code rate of the Walsh codes is $1/T_c =$ 256 MHz. The sampling rate of the DACs is 256 Msps.

An ideal case is evaluated, in which the resolution of the DACs is infinite and the de-modulation mixers are ideal multipliers. Fig. 4 is the array configuration. The eight-element array is linear distributed, and the distance between two adjacent elements is half-wavelength. Fig. 5 shows the beam pattern of the ideal case compared with the reference pattern, which is generated with an ideal conventional DBF transmitter array as shown in Fig. 1. In Fig. 5, the array elements are weighted with Chebyshev weighting, and the direction of the main lobe is tuned to $-20°$. The weighting values for all antenna elements are listed in Table II. It can be seen that in the ideal case, the formed beam pattern is perfectly matched with the reference.

As described in previous section, the key components of the proposed system are the DACs and the de-modulation mixers. Therefore, the requirements of

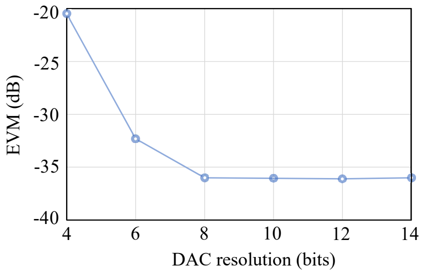

Fig. 7. EVM of systems with different DAC resolutions in 64QAM.

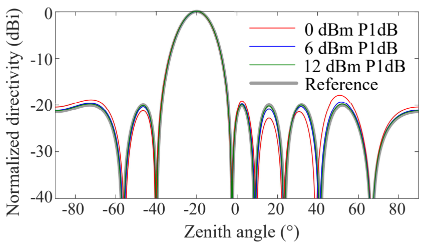

Fig. 8. Beam patterns with different P1dB values of mixers.

TABLE IV
SIDE LOBE ERRORS WITH DIFFERENT P1DB VALUES.

P1dB (dBm)	0	3	6	9	12	15
Side lobe error (dB)	4.36	2.66	1.47	0.77	0.38	0.25

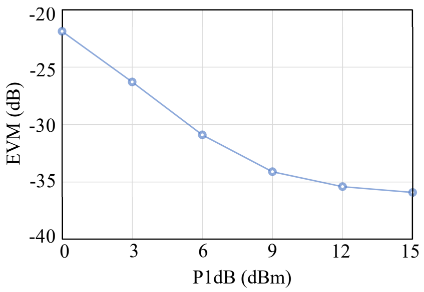

Fig. 9. EVM of different P1dB values in 64-QAM.

these two components are evaluated in the simulation. Fig. 6 shows the beam patterns for systems with different DAC resolutions, all with the same antenna weightings as shown in Table II. The main lobes of the patterns with different DAC resolutions varies slightly. The side lobes errors of the beamforming patterns are listed in Table III. When the resolution is 8-bit or higher, the side lobes errors are smaller than 0.2 dB compared with the reference.

In Fig. 7, the error vector magnitude (EVM) of the transmitted signal is calculated with different DAC resolutions. The modulation method used for $x(t)$ is 64-QAM. The EVM reaches to the minimal at 8-bit DAC resolution.

Another simulation is performed to evaluate the requirements for the de-modulation mixers. The effects of different input 1 dB Gain Compression (P1dB) values of the mixers are evaluated. Fig. 8 illustrates the beam patterns with different input P1dB of the mixers. In the simulation, the input power of the mixers is 0 dBm and the resolution of the DACs is 8 bits. The main lobes of the beam patterns fit the reference very well with different P1dB values. The side lobe errors are below 1 dB as long as the P1dB is larger than 9 dBm.

The EVMs of the transmitted are also calculated with different P1dB values. Fig. 9 shows the EVM results of 64QAM. The EVM is below -35 dB when P1dB is larger than 12 dBm. In hardware implementation, passive mixers can be used to achieve high P1dB.

IV. CONCLUSION

In this paper, a method to reduce the hardware for a DBF transmitter array system has been proposed. By using code-division multiplexing technique, signals from different channels are combined together, which significantly reduce the required number of DACs, as compared with a conventional DBF transmitter array system. After the DAC, signals of different channels are separated through a de-modulation process. Design principle of the proposed code-modulation for hardware reduction in a digital beamforming transmitter system has been described; a system-level simulation has been performed to verify the performance; results show that the beamforming accuracy and signal quality can be maintained with reduced number of DACs in the proposed system.

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