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TR2017-164 November 2017

Abstract

Pulse-width modulation (PWM) has recently become very popular power coding method in all-digital transmitter (ADT) architectures, which employ switch-mode power amplifiers (SMPA) for high power efficiency. Main drawback of PWM is high level of in-band harmonic distortion when digitally implemented, which limits its usage in transceivers realized for software defined radio. Furthermore, upconversion to RF frequency in such ADT systems is commonly done in digital domain. This introduces additional design difficulties, since significant amount of out-of-band harmonic noise, originating from PWM power encoding process, gets folded back into the input signal frequency band, further increasing the total in-band distortion. This paper presents a novel method for simultaneous multilevel power encoding and upconversion to RF frequency, by the means of a delta-sigma M hybrid architecture. It fully exploits time-domain characterization of multilevel carrier-based digital PWM, to both provide optimal parameter selection for delta-sigma M (which gives truly aliasing-free digital PWM), and to utilize harmonic nature of the PWM output for upconversion to digital RF frequency. Experiments with an arbitrary waveform generator are used to demonstrate effectiveness of the proposed novel power encoding scheme. The novel algorithm uses 3-level digital PWM and offers in-band SNR of more than -40dB.

IEEE Asia Pacific Microwave Conference

Simultaneous Power Encoding and Upconversion for All-Digital Transmitters Using Digital PWM

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***Abstract*—Pulse-width modulation (PWM) has recently become very popular power coding method in all-digital transmitter (ADT) architectures, which employ switch-mode power amplifiers (SMPA) for high power efficiency. Main drawback of PWM is high level of in-band harmonic distortion when digitally implemented, which limits its usage in transceivers realized for software defined radio. Furthermore, upconversion to RF frequency in such ADT systems is commonly done in digital domain. This introduces additional design difficulties, since significant amount of out-of-band harmonic noise, originating from PWM power encoding process, gets folded back into the input signal frequency band, further increasing the total in-band distortion. This paper presents a novel method for simultaneous multilevel power encoding and upconversion to RF frequency, by the means of a $\Delta\Sigma$M-PWM hybrid architecture. It fully exploits time-domain characterization of multilevel carrier-based digital PWM, to both provide optimal parameter selection for $\Delta\Sigma$M (which gives truly aliasing-free digital PWM), and to utilize harmonic nature of the PWM output for upconversion to digital RF frequency. Experiments with an arbitrary waveform generator are used to demonstrate effectiveness of the proposed novel power encoding scheme. The novel algorithm uses 3-level digital PWM and offers in-band SNR of more than -40dB.**

I. Introduction

Power efficiency of conventional RF power amplifiers (PA), e.g. class A or B, suffers under modern communication standards, which require signals with highly varying envelopes. Highly efficient switched-mode power amplifiers (SMPA) have shown as a good alternative to traditional PAs [1]- [2]. SMPAs are driven by piece-wise constant signals to achieve high efficiency, which requires some method for resolution reduction (i.e. power encoding) of standard high resolution communication signals.

Pulse-width modulation (PWM) has been one of the most popular methods for power encoding (see e.g. [3] and references therein). It is usually applied on I/Q components of the baseband signal, or the baseband envelope in case of burst mode transmitters [4]. PWM output signal has spectrum of infinite support, and significant amount of spectral noise can fold back into frequency band of interest when such signals are upconverted to RF frequency. Various methods for mitigating this noise folding effect have been proposed in literature [4]-[5]. In [6] authors propose to use harmonic nature of the analog PWM output in order to implement upconversion as part of the PWM process. In this case there are no intermodulation effects that can cause folding of out-of-band noise into the signal band. For transceivers realized for software defined radio, it is advantageous for PWM to be fully digitally implemented (see Fig. 1). But in that case, PWM suffers from high level of in-band harmonic distortion introduced by spectral aliasing effects, which significantly limits its usage in applications [7].

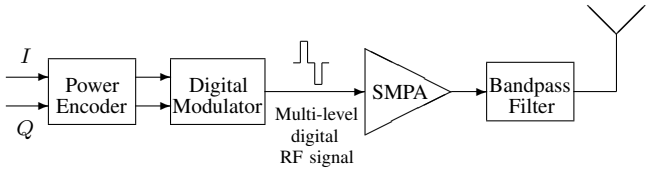

Fig. 1. An example of all-digital transmitter architecture.

In this paper, we propose a novel method for simultaneous multilevel power encoding and upconversion to digital RF frequency using digital PWM. Simple LUT based predistorter is combined with a delta-sigma modulator ($\Delta\Sigma$M) in order to significantly reduce distortion in digital PWM. It fully exploits time-domain characterization of multilevel carrier-based digital PWM, to both provide optimal parameter selection for $\Delta\Sigma$M (which gives truly aliasing-free digital PWM as recently shown in [8]), and to utilize harmonic nature of the PWM output for upconversion to digital RF frequency.

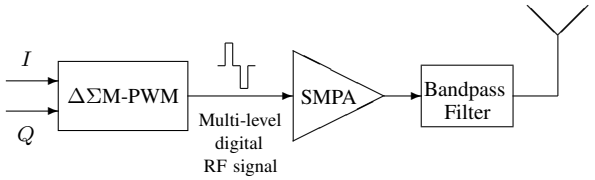

Fig. 2. All-digital transmitter architecture with our proposed power encoding and upconversion scheme.

II. Simultaneous Power Coding and Upconversion Scheme

In this section we describe the proposed digital PWM based simultaneous power coding and upconversion scheme. The abstract block diagram of our novel scheme is shown in Fig. 3. In the following subsections we discuss each of the respective subsystems, and describe the operation of this scheme.

A. Digital PWM

PWM is a well known and widely used modulation method, which has been studied by researchers from various communi-

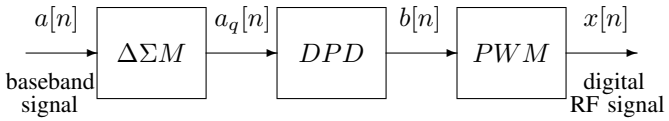

Fig. 3. Abstract block diagram of the proposed simultaneous power encoding and upconversion scheme.

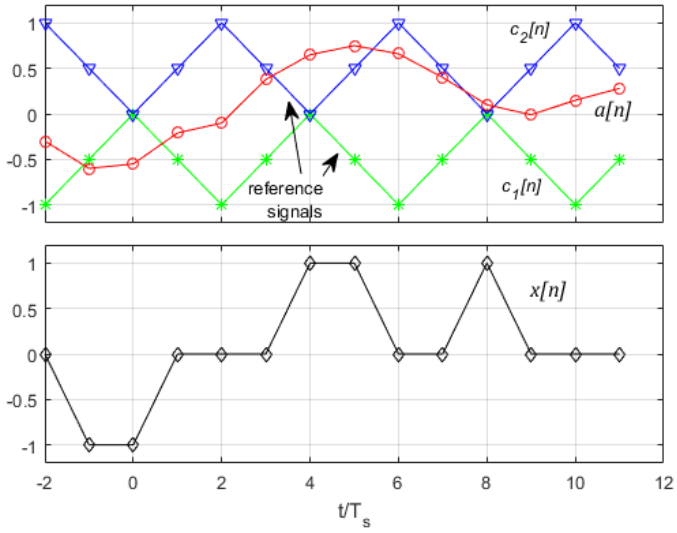

Fig. 4. An example of ouput signal generation in three-level digital PWM.

ties (microwave, power electronics, communications, etc). In this paper, by digital PWM we mean *carrier-based double-edge amplitude-slicing 3-level digital PWM* scheme [8]. Output signal is generated by comparing input to a fixed reference or carrier signal, which in our case is a double-edge sawtooth signal oscillating at frequency f_r (which we call the PWM reference frequency). Two carrier signals are used to produce the PWM output (hence 3 output levels). Digital sampling frequency is denoted as f_s. An example of output signal generation for this PWM scheme is shown in Fig. 4, where $f_s = 4f_r$ (i.e. there are 4 samples per reference period). Both PWM input and output are assumed to be normalized in amplitude to $(-1, 1)$, and the output signal is generated according to the following formula

$$x[n] = \begin{cases} 1, & c_2[n] \le a[n] < 1, \\ 0, & c_1[n] \le a[n] < c_2[n], \\ -1, & -1 < a[n] < c_1[n]. \end{cases} \quad (1)$$

where $c_1[n]$ and $c_2[n]$ are the reference sawtooth signals as denoted in Fig. 4. Without loss of generality, we assume that ratio $f_s/f_r = N$ is an integer, and even more that $N = 9$ (results presented in this paper readily extend to other integer values of N).

Let $a[n]$ and $x[n]$ be the input and output of a 3-level digital PWM, as discussed above. It was shown recently (see [9]) that the output signal $x[n]$ can be expressed as

$$x[n] = a_q[n] + \sum_{k=1}^{N/2} \frac{2\sin(k\pi(a_q[n]+1))}{N\sin(k\pi/N)} \cos\left(\frac{2\pi}{N}kn\right), \quad (2)$$

where $a_q[n] = (\mathbf{Q}a)[n]$ and $\mathbf{Q}$ is a uniform quantizer with dynamic range $(-1, 1)$ and N output levels. Digital PWM can only produce a discrete set of pulse widths, which means that its input signal is effectively quantized to a finite number of quantization levels. Therefore, digital PWM does not perceive the true input signal $a[n]$ but a uniformly quantized version of it (signal $a_q[n]$). This additional quantization process can be seen as time-domain manifestation of the spectral aliasing effects that are inherent to digital PWM operation [9]. As suggested in [8], delta-sigma modulation or some other 'controlled' quantization method should be used to pre-process PWM input signal, so that aliasing-free PWM output is produced. Otherwise, very high oversampling ratio is needed in order to bring the in-band harmonic distortion to an acceptable level. For that reason, we pre-process the baseband signal in such a way that the PWM input appears as uniformly quantized. This is obtained by employing a delta-sigma modulator ($\Delta\Sigma$M) together with an appropriately chosen digital predistortion (DPD) block, as described in the following subsections. In this paper a first order $\Delta\Sigma$M is used for simplicity, but higher order $\Delta\Sigma$M could be chosen as well. In that case an expected improvement in linearity of the overall system is traded for increased implementation complexity, stability issues and lower coding efficiency which are associated with higher order $\Delta\Sigma$M.

1) Upconversion to Digital Carrier: Let f_c be the desired RF frequency. In our proposed system upconversion to a digital carrier is achieved by utilizing harmonic nature of the PWM output (see (2)). For that reason, let us re-write (2) as

$$x[n] = a_q[n] - \frac{2}{N\sin(\pi/N)}\sin(\pi a_q[n])\cos\left(\frac{2\pi}{N}n\right) + \sum_{k=2}^{N/2} \frac{\sin(2k\pi(a_q[n]+1))}{N\sin(k\pi/N)} \cos\left(\frac{2\pi}{N}kn\right). \quad (3)$$

Now, if the reference frequency is set such that $f_r = f_c$ it follows that digital frequency $2\pi/N$ corresponds to analog frequency f_c. That is, by an appropriate modification of the input signal $a[n]$, the second summand in (3) can be considered as a digital cosine modulated by the input signal, or equivalently as an amplitude modulated RF signal (after D/A conversion).

B. Compensation of nonlinearities in PWM

There are two sources of nonlinear distortion in this digital PWM scheme: (1) distortion caused by the quantization process inherent to PWM operation: digital PWM does not see signal $a[n]$ but a quantized version of it, i.e. $a_q[n]$; (2) static nonlinear distortion due to the fact that RF amplitude (i.e. envelope of the first harmonic) is proportional to $\sin(\pi a_q[n])$ and not $a_q[n]$. The first source of distortion can be mitigated by pre-quantization of the baseband signal with an appropriately designed delta sigma modulator (denoted $\Delta\Sigma M$ on the block diagram in Fig. 3). Then, a simple LUT-based pre-distorter (denoted DPD in Fig. 3) can be used to eliminate memoryless distortion in the first harmonic. It is important to emphasize that these two operations (or system blocks) are entangled and their design has to be carried out simultaneously. Let us explain this in more detail.

Let $a_q[n]$ and $b[n]$ be the outputs of $\Delta\Sigma M$ and DPD subsystems, respectively. In other words $a_q[n]$ and $b[n]$ are

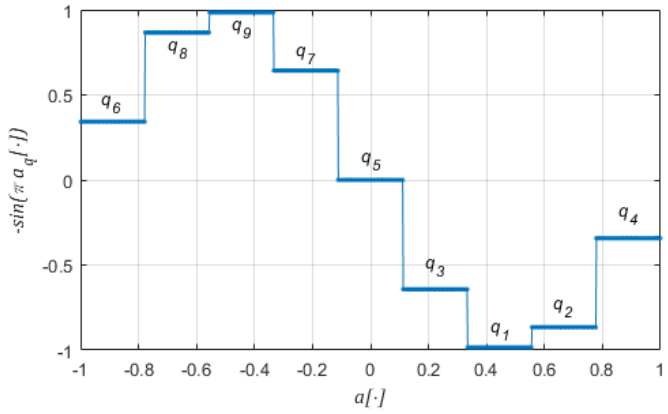

Fig. 5. Characteristic function from PWM input signal $a[\cdot]$ to the envelope of the first harmonic of the PWM output signal.

inputs into DPD and PWM subsystems, respectively (see notation in Fig. 3). As shown in [9], in order to minimize aliasing distortion in digital PWM, signal $b[n]$ has to be quantized exactly according to the inherent PWM quantization process. Therefore, $b[n]$ has to be uniformly quantized on the interval $(-1, 1)$. As can be seen from (3), envelope of the first harmonic of the PWM output is a (memoryless) nonlinear function of the input signal. Due to nature of the nonlinearity in (3) it is clear that normalized inverse sine function should be used in the DPD block, with the corresponding transfer function described as

$$f(\xi) = -\frac{1}{\pi}\arcsin(\xi). \tag{4}$$

Therefore, DPD block has a nonlinear characteristic function. Since signal $b[n]$ has to be uniformly quantized, it follows that $\Delta\Sigma M$ subsystem has to act as a non-uniform quantizer, where its exact levels are defined by the DPD characteristic function (or more precisely the inverse thereof). This characteristic function cannot be applied on $\Delta\Sigma M$ output without an appropriate reshuffling of the input signal values, due to non-monotonicity of the sine function on the interval $(-\pi, \pi)$. This is depicted in Fig. 5. As signal $a[\cdot]$ goes monotonically over interval $(-1, 1)$, the envelope of the first harmonic oscillates in the same interval, assuming finitely many levels. Therefore, our scheme would produce a non-distorted envelope of the first harmonic if the non-uniform quantizer in the $\Delta\Sigma M$ subsystem assumes levels $\{q_1, \ldots, q_9\}$ as shown in Fig. 5. Since quantization bins in signal $a[n]$ do not map monotonically to levels q_i, an appropriate reshuffling of amplitude values has to be performed in the DPD block.

III. Experimental Performance Evaluation

Measurements have been carried in order to experimentally evaluate the proposed simultaneous power encoding and upconversion scheme. Performance of the system is measured in terms of achieved in-band signal-to-noise ratio (SNR), and measured for two different input signals. The in-phase component of a 64QAM signal with 5 MHz and 10 MHz bandwidth has been used for evaluation, with carrier frequencies of 1 GHz and 2 GHz, respectively. In both cases, PWM frequency is equal to the carrier frequency, and OSR is 9, thus giving the sampling frequency of 9 GS/s and 18 GS/s, respectively. Number of output levels of PWM is set to 3, and the number of $\Delta\Sigma$M output levels is therefore 9. In order to simplify system design, a first order $\Delta\Sigma$M is used.

Matlab simulated output signals file is loaded into an arbitrary waveform generator (AWG-34G from Micram Instruments) to generate the signals. Keysight EXA 9010A signal analyzer is used to measure the spectrum. Figs. 7 and 9 show the measured spectrum of the input signals with 5 MHz bandwidth at 1 GHz and 10 MHz bandwidth at 2 GHz, respectively. Figs. 8 and 10 show the zoom-in spectrum of each signal. Measured in-band SNRs are -45.6dB and -40.4dB respectively, where the baseband input signals have SNR of roughly -50dB.

IV. Conclusion

A highly linear method for simultaneous multilevel power encoding and upconversion to digital RF frequency has been demonstrated. It employs a $\Delta\Sigma$M-PWM hybrid architecture, with an additional pre-emphasis subsystem positioned between $\Delta\Sigma$M and PWM blocks, in order to correct for the memoryless nonlinear distortion introduced by the PWM. In addition, parameters of the $\Delta\Sigma$M are chosen in optimal way in order to minimize output in-band SNR, i.e. to mitigate harmonic distortion caused by spectral aliasing effects inherent to digital PWM operation. Future work will include combining both I and Q signal paths, and tailoring PWM method so to optimize power efficiency as well as in-band SNR.

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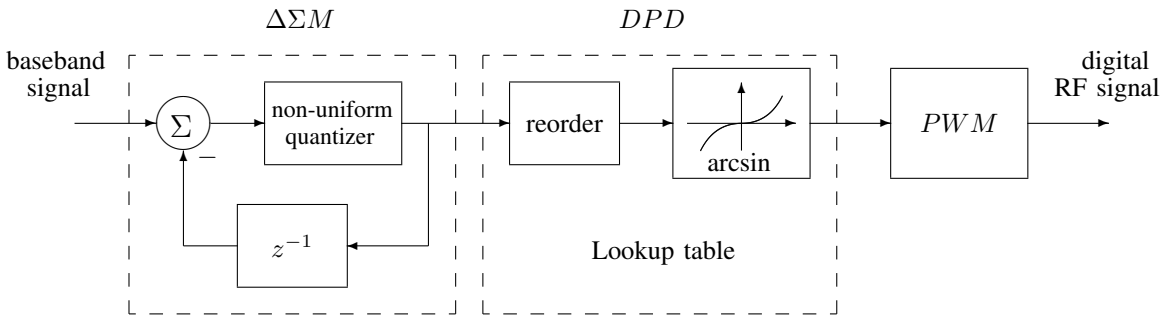

Fig. 6. Detailed block diagram of the proposed simultaneous power coding and upconversion scheme.

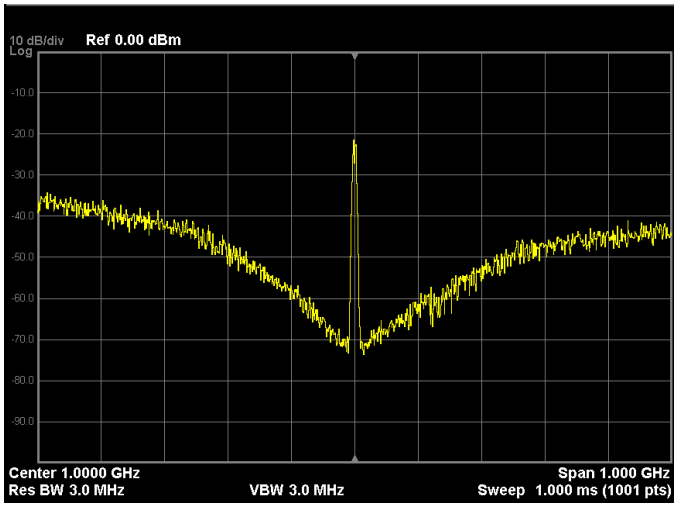

Fig. 7. Measured wideband spectrum of the PWM output for the 5 MHz bandwidth signal.

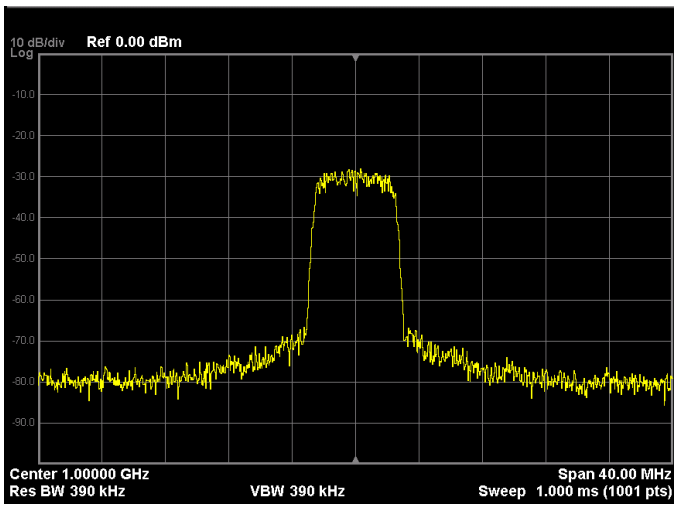

Fig. 8. Measured passband spectrum of the PWM output for the 5 MHz bandwidth signal.

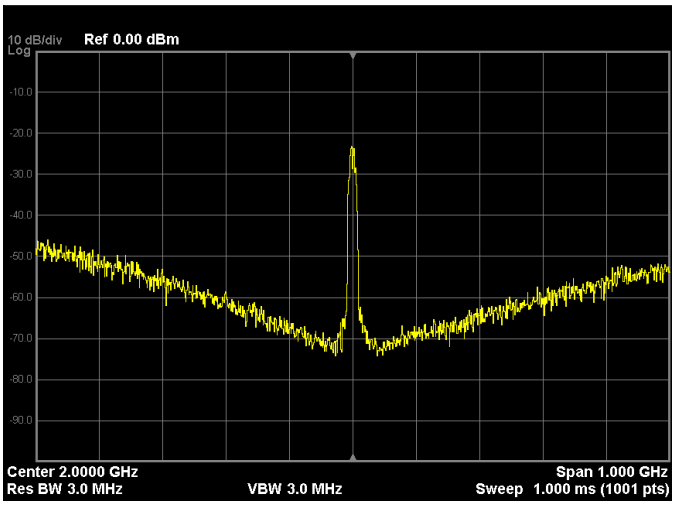

Fig. 9. Measured wideband spectrum of the PWM output for the 10 MHz bandwidth signal.

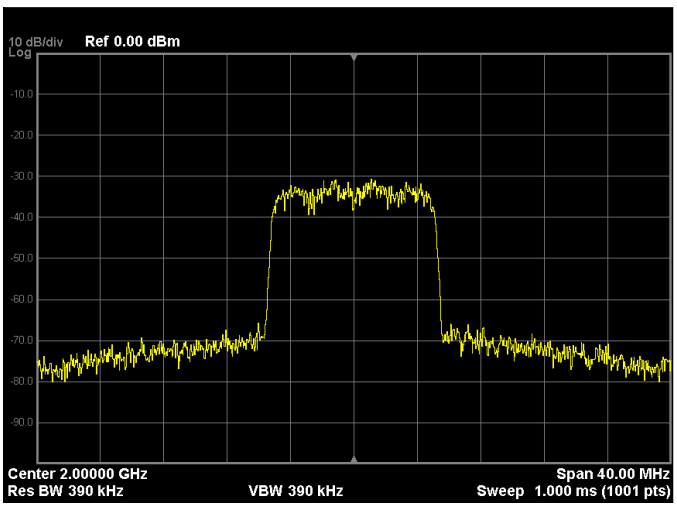

Fig. 10. Measured passband spectrum of the PWM output for the 10 MHz bandwidth signal.